High Accuracy, Full Protection & Diagnostics, Constant-Current RGB LED Driver with Sleep-Mode

1. FEATURES

- 33 Constant-Current-Sink Output Channels
  - 30-mA Maximum Output Current
  - 5-V Maximum Output Voltage
  - 3 Output Groups: OUTRn, OUTGn, OUTBn
- Output Current Adjustment
  - 7-Bit Dot Correction for Each Channel
  - 8-Bit Intensity Control for Each Group
- Integrated PWM Grayscale Generator
  - PWM Dimming for Each Individual Channel
  - Adjustable Global Grayscale Mode: 12-Bit, 10-Bit, 8-Bit
- Protection and Diagnostics
  - LED-Open Detection, LED-Short Detection, Output Short-to-GND Detection
  - Adjacent-Pin Short Detection
  - Pre-Thermal Warning, Thermal Shutdown
  - IREF Resistor Open- and Short-Detection and -Protection
  - Negate Bit Toggle for GCLK Error Detect and LOD_LSD Register Error Check
  - LOS_LSF Circuit Self-Test
- Programmable Output Slew Rate
- Output Channel Group Delay
- Support Serial Data Interface Communication from Simple 8-bit MCU
- Support Sleep Mode with supply current below 100uA
- High Accuracy: Typical +/-7% per channel

2. APPLICATIONS

- Automotive Interior & RGB Ambient Lighting
- Automotive Center Stack Display
- Automotive Shift-by-Wire and Gear Shifter
- Automotive Faceplate
- Automotive Local Dimming Display

3. GENERAL DESCRIPTION

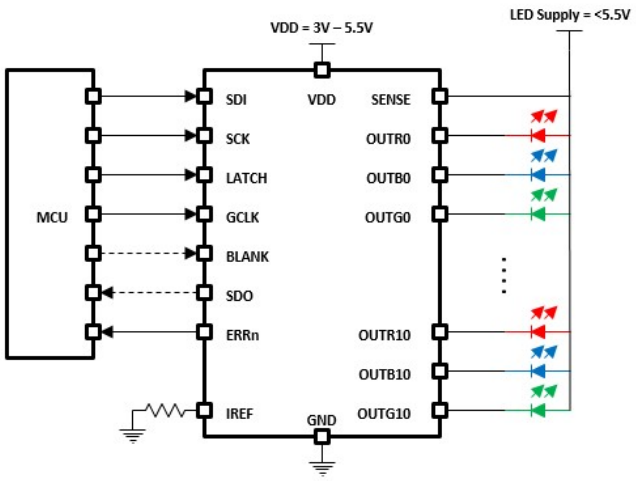
The HT1388 is designed for driving 33-channel LEDs Driver. It can supply a maximum 30mA constant output current set by an external resistor. The device has a 7-bit dot correction for each output. The device also has an 8-bit intensity control for the outputs of each color group.

A 12-, 10-, or 8-bit grayscale control adjusts the intensity of each output. The device has circuits that sense faults in the system, including LED faults, adjacent-pin short faults, reference-resistor faults, and etc. Two slew rate control can be programmed for adjustment to get the largest decrease in system noise. There is an interval between the changes of output level from on LED group to a different one. This interval helps to decrease the starting electrical current. The SDI and SDO pins let more than one device be connected in series for control through one serial interface.

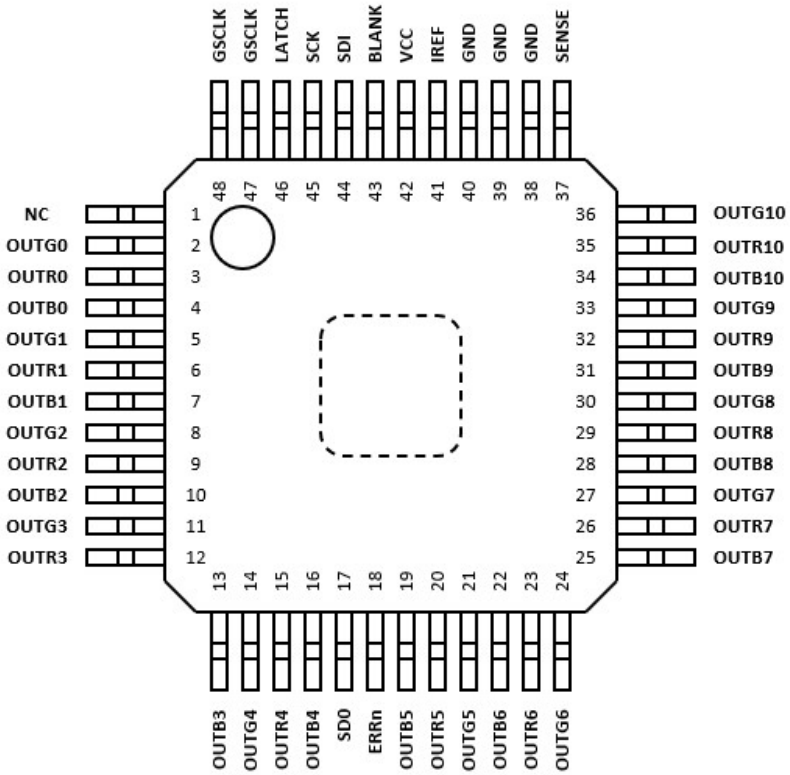
4. PART NUMBER INFORMATION

PART NO.	PACKAGE
HT1388FP	eQFP48
HT1388FN	QFN48

5. TYPICAL APPLICATION



6. PIN CONFIGURATION AND DESCRIPTIONS



Pin assignment of HT1388FP

Pin Descriptions

Pin No.	Pin Name	I/O	Description
44	SDI	I	Serial data-in pin
45	SCK	I	Data-shift clock-input pin
46	LATCH	I	Latch-enable input pin
47,48	GCLK	I	Clock input for grayscale PWM counter. These two pins are connected together internally.
2,5,8,11,14,21,24,27,30,33,36	OUTG0-10	O	Constant-current outputs for color Green
3,6,9,12,15,20,23,26,29,32,35,	OUTR0-10	O	Constant-current outputs for color Red
4,7,10,13,16,19,22,25,28,31,34	OUTB0-10	O	Constant-current outputs for color Blue

Pin Descriptions (continued)

Pin No.	Pin Name	I/O	Description
38,39,40	GND	-	Power ground
37	SENSE	I	Connect to LED supply for LED diagnostics
41	IREF	I	Reference-current pin for setting the full-scale output current
42	VCC	-	Power supply pin
43	BLANK	I	Blank all outputs. BLANK low for
18	ERRn	O	Open-drain error feedback
17	SDO	O	Serial data-out pin
1	NC	-	Not connected
-	Thermal pad	-	Connect to ground to improve thermal performance

7. SPECIFICATIONS

7.1. Absolute Maximum Ratings

	PIN Name	Symbol	Value	Unit
Input Voltage	V_{CC}		-0.3 to 6	V
	SENSE		-0.3 to 6	V
	BLANK, GCLK, LATCH, SCK, SDI		-0.3 to V_{CC} + 0.3	V
Output Voltage	ERRn, IREF, SDO		-0.3 to V_{CC} + 0.3	V
	OUTR0-10, OUTG0-10, OUTB0-10		-0.3 to 6	V
Output Current	OUTR0-10, OUTG0-10, OUTB0-10		0 to 30	mA
Junction temperature range		T_J	-40 to +140	°C
Maximum soldering temperature (at leads, 10sec)		T_{LEAD}	+300	°C
Storage temperature range		T_S	-55 to +150	°C
Junction to case(bottom) thermal resistance		θ_{JC}	30	°C /W

Remarks: 1) All voltages are with respect to GND unless otherwise noted.

7.2. ESD Ratings

		VALUE	Unit
HT1388FN (QFN48 package)			
Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V

7.3. Recommended Operating Conditions

		MIN	NOM	MAX	Unit
V_{CC}	Supply input voltage	3		5.5	V
V_{SENSE}	LED supply voltage			5.5	V
Vo	Output voltage			5.5	V
V_{IL}	Input logic-low voltage	0		0.3*V_{CC}	V
V_{IH}	Input logic-high voltage	0.7*V_{CC}		V_{CC}	V
I_{OH}	High-level output source current at SDO			1	mA
I_{OL}	Low-level output sink current at SDO			1	mA
	Low-level output sink current at ERRn			5	mA
I_O	Constant output sink current	2		30	mA
T_A	Operating ambient temperature	-40		125	°C
T_J	Operating junction temperature	-40		150	°C

7.4. Electrical Characteristics

V_{CC} = 5V, T_J=25°C, V_{SENSE} = 5V, GS=FFFh, BC=FFh, DC=7Fh with high DC_RANGE (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{CC}	Supply Current	SDI, SCK, LATCH=L, BLANK=L, GCLK=L, V_{OUT}=1V, I_{OUT}=2mA		6		mA
		SDI, SCK, LATCH=L, BLANK=L, GCLK=L, V_{OUT}=1V, I_{OUT}=20mA		9		
		SDI, SCK, LATCH=L, BLANK=H, GCLK=8Mhz, V_{OUT}=1V, I_{OUT}=20mA, auto-repeat on		10		
		SDI, SCK, LATCH=L, BLANK=H, GCLK=8Mhz, V_{OUT}=1V, I_{OUT}=30mA, auto-repeat on		16		
$I_{SHUTDOWN}$	Shutdown Current				100	uA
LOGIC INPUTS (SDI, SCK, LATCH, GCLK, BLANK)						
I_{lkg}	Input leakage current	At SDI, SCK, LATCH, with V_I=V_{DD};		1		uA
R_{pd}	Pull down resistance at BLANK, GCLK			500		kΩ
CONTROL OUTPUTS (IREF, ERRn, SDO)						
V_{IREF}	IREF voltage	R_{IREF} =1600Ω		1.220		V
V_{OH}	High-level output voltage	At SDO, I_{OH} = -1mA	V_{DD}-0.4			V
V_{OL}	Low-level output voltage	At SDO, I_{OL} = 1mA			0.4	V
V_{ERRn}	ERRn pin open-drain voltage drop	I_{ERRn} = 4mA			0.1*V_{DD}	V
I_{LKG_ERR}	ERRn pin leakage current	V_{ERRn} = 5V		1		uA
OUTPUT STAGE						
$V_{(OUT,min)}$	Minimum output voltage	Vcc = 3V, I_{OUT} = 30mA			0.7	V
$K_{(OUT)}$	Current Gain	I_{OUT} = 30mA		40		mA/mA
$I_{LKG(OUT)}$	Output leakage current	BLANK=L, Vout=5V			0.1	uA
CHANNEL ACCURACY						
$I_{(OUT)}$	Constant output current	Vout=1V, R_{IREF} = 24 kΩ		1.8		mA
		Vout=1V, R_{IREF} = 1.6 kΩ		30		
		Vout=1V, R_{IREF} open/ short		10		

Electrical Characteristics (continued)

V_{CC} = 5V, T_J=25°C, V_{SENSE} = 5V, GS=FFFh, BC=FFh, DC=7Fh with high DC_RANGE (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUTS (SDI, SCK, LATCH, GCLK, BLANK)						
$\Delta I_{(Ch-Ch)}$	Current accuracy (channel-to-channel in same group)	Vout = 1V, Iout = 30mA	-5%		5%	
$\Delta I_{(Dev-Dev)}$	Current accuracy (device-to-device)	Vout = 1V, Iout = 30mA	-5%		5%	
$\Delta I_{(Ch-Ideal)}$	Current accuracy (channel-to-ideal output)	Vout = 1V, Iout = 30mA	-5%		5%	
$\Delta I_{(OUT-VDD)}$	Line Regulation	Vout = 1V, Iout = 30mA Vcc = 3V to 5.5V	-1%		1%	%/V
$\Delta I_{(OUT-VOUT)}$	Load Regulation	Vcc = 3V, Iout = 30mA Vout = 1V to 3V	-1%		1%	%/V
PROTECTION CIRCUITS						
V_{LOD1}	LED open-circuit detection low threshold	LOD_VOLTAGE = 0b		0.3		V
V_{LOD2}	LED open-circuit detection high threshold	LOD_VOLTAGE = 1b		0.5		V
V_{LSD1}	LED short-circuit detection low threshold	LSD_VOLTAGE = 0b		V_{SENSE} - 0.3		V
V_{LSD2}	LED short-circuit detection high threshold	LSD_VOLTAGE = 1b		V_{SENSE} - 0.7		V
I_{IREF_OC}	R_{IREF} open-circuit detection threshold	V_{CC} = 5V		10		uA
$I_{IREF\_OC\_HYS}$	R_{IREF} open-circuit detection hysteresis	V_{CC} = 5V		5		uA
I_{IREF_SC}	R_{IREF} short-circuit detection threshold	V_{CC} = 5V		2.4		mA
$I_{IREF\_SC\_HYS}$	R_{IREF} short-circuit detection hysteresis	V_{CC} = 5V		0.3		mA
T_{PTW}	Pre-Thermal warning flag threshold	Junction temperature		135		ºC
T_{PTW_HYS}	Pre-Thermal warning flag hysteresis	Junction temperature		10		ºC
T_{TEF}	Thermal error flag threshold	Junction temperature		160		ºC
T_{TEF_HYS}	Thermal error flag hysteresis	Junction temperature		10		ºC

7.5 Timing Requirements

V_{CC} = 3 V to 5.5 V, TJ=–40°C to 150°C.

		MIN	NOM	MAX	UNIT
$f_{CLK(SCK)}$	SCK data-shift clock frequency			4	MHz
$f_{CLK(GCLK)}$	GCLK grayscale clock frequency			8	MHz
t_{WH0}	SCK high pulse duration	60			ns
t_{WL0}	SCK low pulse duration	60			ns
t_{WH1}	LATCH high pulse duration	80			ns
t_{WL1}	LATCH low pulse duration	80			ns
t_{WL2}	BLANK pulse duration	T_{GCLK}			ns
t_{WH3}	GCLK high pulse duration	40			ns
t_{WL3}	GCLK low pulse duration	40			ns
t_{SU0}	SDI - SCK↑ setup time	55			ns
t_{SU1}	BLANK↑– GCLK↑ setup time	60			ns
t_{SU2}	LATCH↑ – SCK↑ setup time	200			ns
t_{SU3}	LATCH↑ for GS data – GCLK↑ when display timing reset mode is disabled, setup time	90			ns
t_{SU4}	LATCH↑ for GS data – GCLK↑ when display timing reset mode is enabled, setup time	150			ns
t_{H0}	SCK↑– SDI hold time	55			ns
t_{H1}	SCK↑– LATCH↑ hold time	85			ns
t_{H2}	SCK↑– LATCH↓ hold time	55			ns
t_{RI0}	SDI, SCK, LATCH rise time			50	ns
t_{RI1}	GCLK rise time			30	ns
t_{FI0}	SDI, SCK, LATCH fall time			50	ns
t_{FI1}	GCLK fall time			30	ns

7.6 Switching Characteristics

Over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ro0}	Rise time from 10% V_{SDO} to 90% V_{SDO}			60		ns
t_{ro1}	Rise time from 10% V_{OUT} to 90% V_{OUT}	IOUT = 30mA, SLEW_RATE = 0b		220		ns
		IOUT = 30mA, SLEW_RATE = 1b		120		
t_{fo0}	Fall time from 90% V_{SDO} to 10% V_{SDO}			60		ns
t_{fo1}	Fall time from 90% V_{OUT} to 10% V_{OUT}	IOUT = 30mA, SLEW_RATE = 0b		220		ns
		IOUT = 30mA, SLEW_RATE = 1b		120		
t_{pd0}	Propagation delay, SCK↑ to SDO			140		ns
t_{pd1}	Propagation delay, LATCH↑ to SDO			180		ns

Switching Characteristics (continued)

Over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd2}	Propagation delay, BLANK↓ to OUTR0, -G0, -B0, -R6, -G6, -B6 off			100		ns
t_{pd3}	Propagation delay, GCLK↑ to OUTR0, -G0, -B0, -R6, -G6, -B6 on			100		ns
t_{pd4}	Propagation delay, GCLK↑ to OUTR1, -G1, -B1, -R7, -G7, -B7 on			150		ns
t_{pd5}	Propagation delay, GCLK↑ to OUTR2, -G2, -B2, -R8, -G8, -B8 on			200		ns
t_{pd6}	Propagation delay, GCLK↑ to OUTR3, -G3, -B3, -R9, -G9, -B9 on			250		ns
t_{pd7}	Propagation delay, GCLK↑ to OUTR4, -G4, -B4, -R10, -G10, -B10 on			300		ns
t_{pd8}	Propagation delay, GCLK↑ to OUTR5, -G5, -B5 on			350		ns
t_{pd9}	Propagation delay, LATCH↑ to V_{OUT}			80		ns
t_{pd10}	Propagation delay, LATCH↑ to APS_FLAG change	APS_CURRENT = 0b		10		us
		APS_CURRENT = 1b		20		
t_{pd11}	Propagation delay, LATCH↑ to LOD_LSD_FLAG change	No failure in LOD_LSD detector circuit		10		us

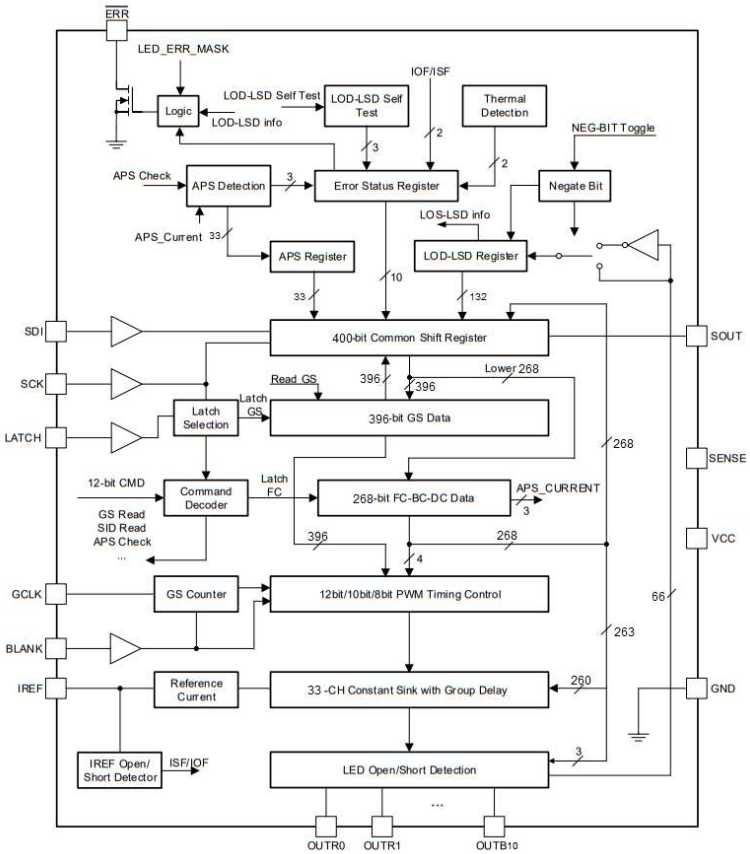
8 Detailed Description

8.1.1 Overview

In automotive indicator and local dimming backlighting applications, the demand for multi-channel constant-current LED drivers are increasing to achieve uniformity of LED brightness and color temperature. System-level safety considerations require fault-detection capability and device self-check features.

The HT1388 device is an automotive 33-channel constant-current RGB LED driver with LED diagnostics. The HT1388 device provides up to 30-mA output current set by an external resistor. The current can be adjusted by 7-bit dot correction with two subranges for individual output and an 8-bit brightness control for the outputs of each color group. The brightness can be adjusted individually for each channel through a 12-,10-, or 8-bit grayscale control. Fault-detection circuits are available to detect system faults including LED faults, adjacent-pin short faults, reference-resistor faults, and more. Negate bit toggle and LOD-LSD self-test provide a device self-check function to improve system reliability. Configurable slew-rate control optimizes the noise generation of the system and improves the system EMC performance. Output-channel group delay helps to reduce inrush current to optimize the system design. The SDI and SDO pins allow more than one device to be connected in a daisy chain for control through one serial interface.

8.1.2 Functional Block Diagram



8.2 Feature Description

8.2.1 Maximum Constant-Sink-Current Setting

LED full-scale current can be programmed using an external resistor connected between the IREF pin and GND. The R_{IREF} resistor value is calculated with the following formula.

$$R_{IREF} = K \times \frac{V_{IREF}}{I_{(OUT)max}}$$

where

- V_{IREF} is the reference voltage
- K is the IREF-current to output-current ratio
- $I_{(OUT)max}$ is full-scale current for each output (1)

Figure 15 shows the reference resistor calculation curve.

8.2.2 Brightness Control and Dot Correction

The HT1388 device implements an 8-bit group brightness control (BC) and 7-bit individual dot correction (DC) to calibrate the output current. The 33 output channels are divided into three groups: OUTRn, OUTGn, and OUTBn. Each group contains 11 output channels. There are two configurable ranges for the DC value of each group. One is the low DC range with output current from 0 to 66.7% $I_{(OUT)max}$. The other is the high DC range with output current from 33.3% $I_{(OUT)max}$ to 100% $I_{(OUT)max}$. The IREF resistor, BC, DC, and DC range together determine the channel output current, as shown in Figure 21. Equation 2 and Equation 3 are the detailed output current calculation formulas.

Equation 2 determines the output sink current for each color group when DC is in the high adjustment range.

$$I_{OUT} = \left(\frac{1}{3} \times I_{(OUT)max} + \frac{2}{3} \times I_{(OUT)max} \times \frac{DC}{127}\right) \times \frac{BC}{255} \quad (2)$$

Equation 3 determines the output sink current for each color group when DC is in the low adjustment range.

$$I_{OUT} = \frac{2}{3} \times I_{(OUT)max} \times \frac{DC}{127} \times \frac{BC}{255} \quad (3)$$

Feature Description (continued)

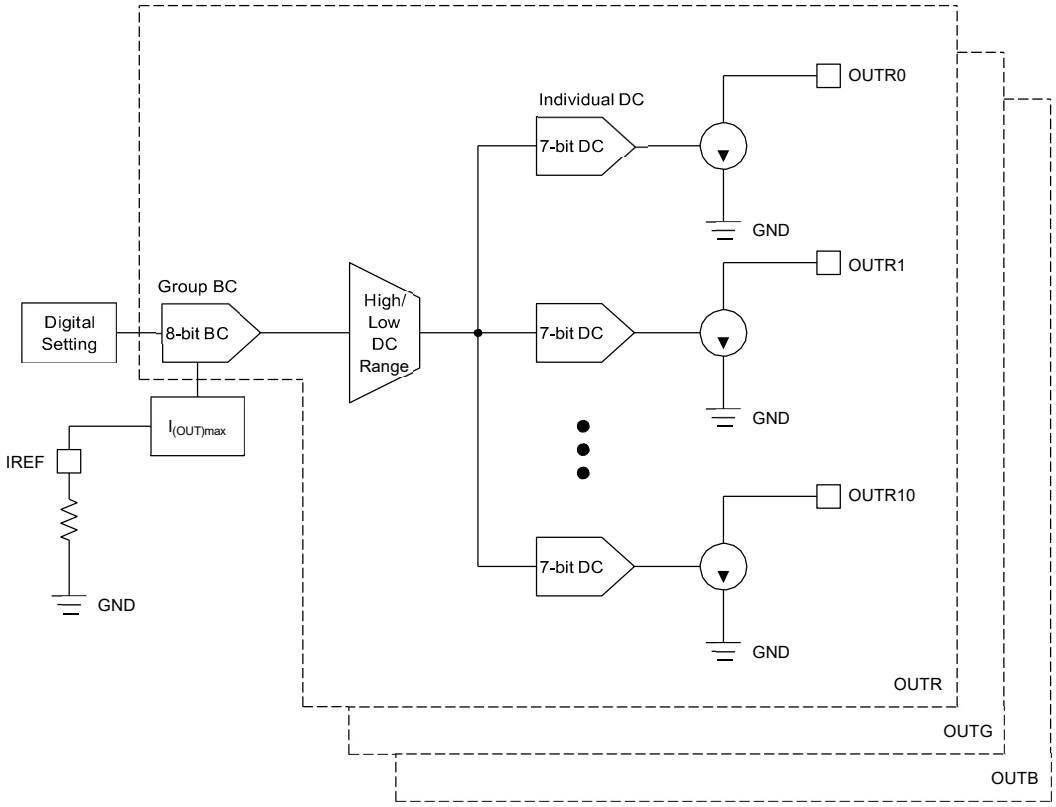


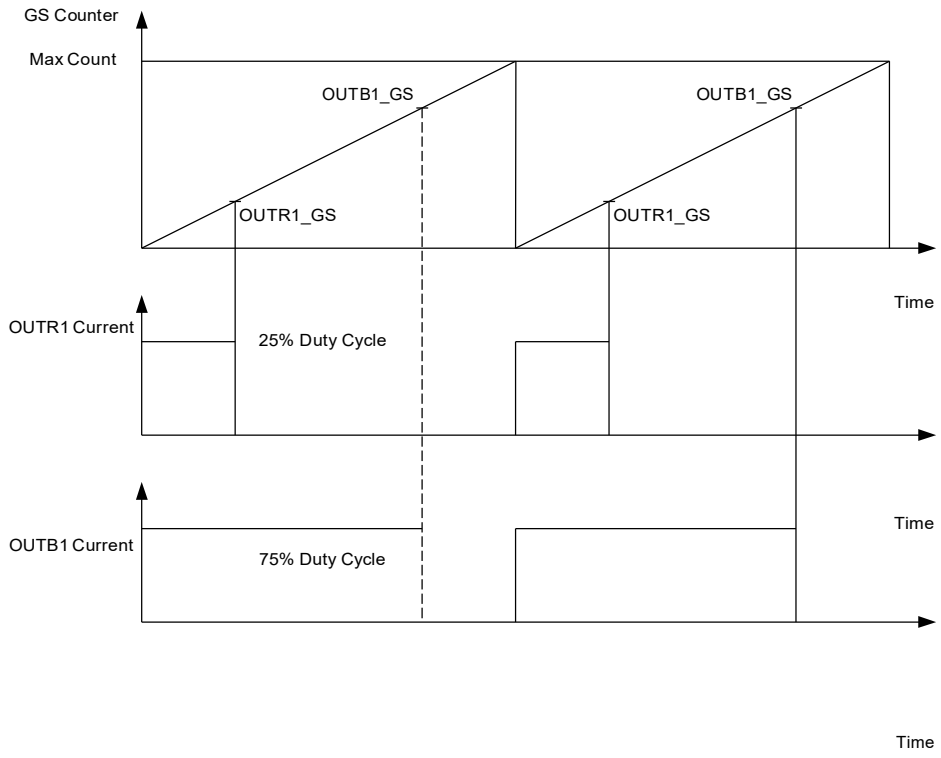
Figure 21. Brightness Control and Dot Correction Block Diagram

8.2.3 Grayscale Configuration

The HT1388 device implements a grayscale configuration function to realize the individual PWM dimming function for the output channels. The grayscale has three global configuration modes, 12-bit, 10-bit and 8-bit. The GCLK input provides the clock source for the internal PWM generator. The GS counter counts the GCLK number and compares the number with the channel grayscale register value. The output channel turns off when the GS counter value reaches the grayscale register value. Figure 22 shows the detailed block diagram of the PWM generator.

To restart a new PWM cycle, users can use two methods. One is to toggle the BLANK pin after the GS counter reaches the maximum count value, because BLANK low resets the GS counter and BLANK high restarts the GS counter. Another is to pull BLANK high and set the AUTO_REPEAT&TIMING_RESET register bit to 1. The PWM starts a new cycle automatically after the GS counter reaches the maximum count value.

Feature Description (continued)



12-bit GS mode, Max Count = 4096
10-bit GS mode, Max Count = 1024
8-bit GS mode, Max Count = 256

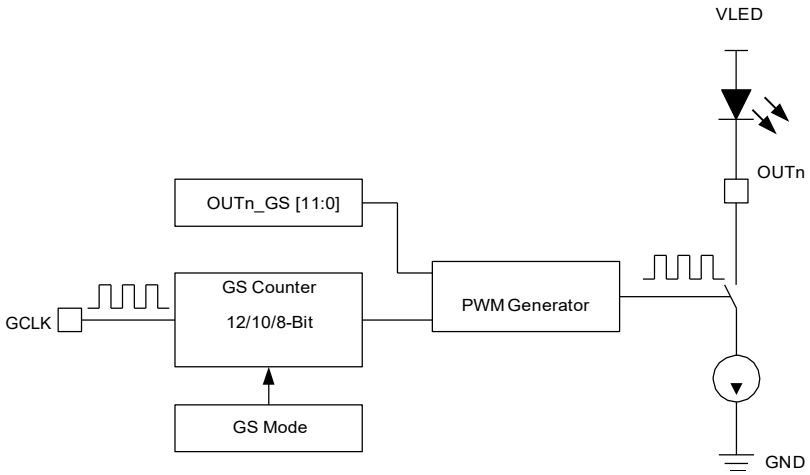


Figure 22. PWM Generator

8.3.3.1 PWM Auto Repeat

The PWM auto repeat function is configured by the AUTO_REPEAT bit. The AUTO_REPEAT bit is 0 by default, and the PWM auto repeat function is disabled under this condition. The PWM cycle only executes once, so users must toggle BLANK to restart a new PWM cycle. Figure 11 and Figure 12 show the PWM operation in this mode. When the AUTO_REPEAT bit is 1, the PWM auto repeat function is enabled. The PWM cycle automatically repeats as long as BLANK is high and GCLK is present, as shown in Figure 13.

Feature Description (continued)

8.3.3.2 PWM Timing Reset

PWM timing reset function is configured by the TIMING_RESET bit. The PWM timing reset function can restart a PWM cycle with newly configured duty-cycle after a GS data write. The TIMING_RESET bit is 0 by default, The PWM timing reset function is disabled in this condition. The PWM duty cycle is not influenced by a GS data write. The newly configured PWM duty-cycle only is valid after the current PWM cycle finishes. When the TIMING_RESET bit is 1, the PWM timing reset function is enabled, and the PWM cycle restarts with the new PWM duty-cycle immediately after the GS data write.

8.3.4 Diagnostics

The HT1388 device integrates a full LED diagnostics functionality, such as LED open detection (LOD), LED short detection (LSD), and output short-to-GND detection (OSD), which improves the system safety.

8.3.4.1 LED Diagnostics

An LOD-LSD detection circuit compares the output voltage with the LOD threshold and LSD threshold, and the output results show in Table 1.

Table 1. LOD-LSD Detection

OUTPUT VOLTAGE CONDITION	DETECTOR OUTPUT BIT VALUE	
	LOD	LSD
V_{OUTn} < LOD_VOLTAGE	1	0
LOD_VOLTAGE < V_{OUTn} < LSD_VOLTAGE	0	0
V_{OUTn} > LSD_VOLTAGE	0	1

The LOD threshold can be configured by the LOD_VOLTAGE bit. The threshold is 0.3 V when LOD_VOLTAGE = 0, and the threshold is 0.5 V when LOD_VOLTAGE = 1.

Table 2. LOD Threshold

LOD_VOLTAGE BIT	LOD THRESHOLD
0 (Default)	0.3 V
1	0.5 V

LSD threshold is configured by the LSD_VOLTAGE bit. The threshold is V_{VSENSE} – 0.3 V when LSD_VOLTAGE = 0, and the threshold is VSENSE – 0.7 V when LSD_VOLTAGE = 1.

Table 3. LSD Threshold

LSD_VOLTAGE BIT	LSD THRESHOLD
0 (Default)	V_{SENSE} – 0.3 V
1	V_{SENSE} – 0.7 V

There are two sets of LOD-LSD registers in the device. One is the LOD1-LSD1 registers, another is the LOD2-LSD2 registers. Each group of registers consists of 33 bits of LOD data and 33 bits of LSD data, corresponding to 33 channel outputs. The device updates the LOD1-LSD1 registers at the 9th GCLK rising edge. The device updates the LOD2-LSD2 registers the Nth GCLK rising edge. N is the maximum GCLK number in a PWM period minus 1, see Table 4.

To detect all kinds of LED faults, the output channel should turn ON at the 9th GCLK rising edge, and turn OFF at the Nth GCLK rising edge.

The device integrates an internal pullup circuit for LED diagnostics, shown in Figure 23. The circuit turns off during the channel on-state, but turns on to charge the output pin during the channel off-state. For an LED-short fault, both LSD1 and LSD2 are 1. For an LED-open fault, both LOD1 and LSD2 are 1. For an output short-to-GND fault, both LOD1 and LOD2 are 1. Table 5 shows the details.

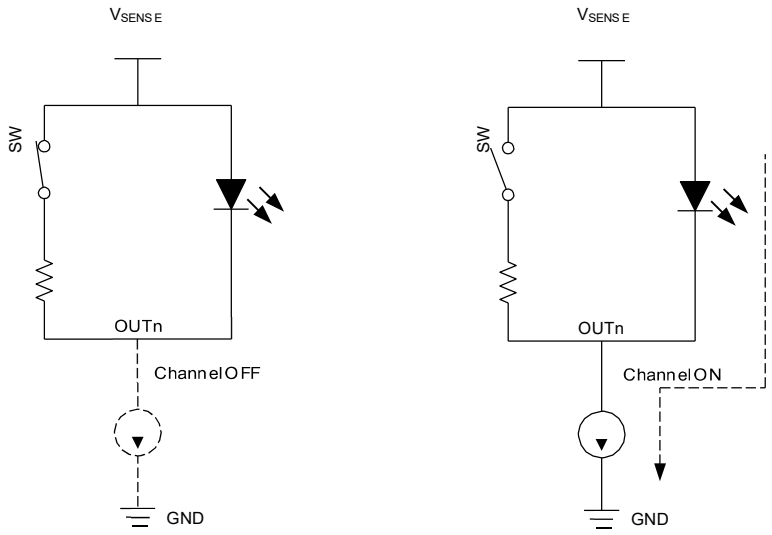


Figure 23. Internal Pullup Circuit

Table 4. LOD-LSD Register Latch Timing

GS COUNTER MODE	LOD1-LSD1	LOD2-LSD2
12-bit	9th GCLK rising edge	4095th GCLK rising edge
10-bit	9th GCLK rising edge	1023rd GCLK rising edge
8-bit	9th GCLK rising edge	255th GCLK rising edge

Table 5. LED Status Lookup Table

LED STATUS	LOD-LSD RESULT			
	LOD1-LSD1 UPDATED AT 9th GCLK		LOD2-LSD2 UPDATED AT Nth GCLK(1)	
LED Ok	LOD1	0	LOD2	0
	LSD1	0	LSD2	1
LED open	LOD1	1	LOD2	0
	LSD1	0	LSD2	1
LED short	LOD1	0	LOD2	0
	LSD1	1	LSD2	1
Output short-to-GND	LOD1	1	LOD2	1
	LSD1	0	LSD2	0

(1) N = 4095 for 12-bit GS mode, 1023 for 10-bit GS mode, 255 for 8-bit GS mode

In some cases, users may need to turn off output channels before the 9th GCLK to disable output channels, or turn on output channels at Nth GCLK to get more brightness. LOD_LSD faults are reported as shown in Table 6. Users can ignore the fault according to the GS register setting value.

Table 6. PWM Status Lookup Table

	LOD-LSD RESULT			
PWM STATUS	**LOD1-LSD1 UPDATED AT 9th GCLK**		**LOD2-LSD2 UPDATED AT Nth GCLK(1)**	
PWM OK	LOD1	0	LOD2	0
	LSD1	0	LSD2	1
Channel off before 9th GCLK	LOD1	0	LOD2	0
	LSD1	1	LSD2	1
Channel on at Nth GCLK	LOD1	0	LOD2	0
	LSD1	0	LSD2	0

(1) N = 4095 for the 12-bit GS mode, 1023 for the 10-bit GS mode, 255 for the 8-bit GS mode

The LOD_LSD status is updated every PWM cycle. Figure 14 is an example of the LOD-LSD register update timing for the 12-bit GS mode.

8.3.4.2 Adjacent-Pin-Short Check

The device implements the APS check function to detect the adjacent-pin short failures during system initialization. TI recommends to do an APS check when channels are all off. The APS check can be executed by writing the APS check command.

If there is no adjacent-pin short failure, the device passes the APS check and 011b is latched into APS FLAG in the error status register. The 33-bit APS register is 0. If there are two adjacent pins shorted, 110b is latched into APS_FLAG in the error status register. The corresponding bit in the APS register is set to 1. Users can read out the 33-bit data from the APS register to check which channel has the APS failure. Table 7 shows the details of the APS_FLAG and APS register. Table 8 shows the bit arrangement of the APS register. To read this APS information, see Table 22.

Table 7. APS Flag and APS Register

REGISTER	VALUE	DESCRIPTION
APS_FLAG	011b	Pass, no adjacent pins short
	110b	Fail, adjacent pins short
Bit in APS register (33-bit total)	0b	This OUTn pin is not shorted with other pins
	1b	This OUTn pin is shorted with other pins

Table 8. Bit Arrangement of the APS Register

BIT OF APS REGISTERS	CORRESPONDING OUTPUTS
Bit 32	OUTB10
Bit 31	OUTB9
Bit 30	OUTB8
Bit 29	OUTB7
Bit 28	OUTB6
Bit 27	OUTB5
Bit 26	OUTB4
Bit 25	OUTB3
Bit 24	OUTB2
Bit 23	OUTB1
Bit 22	OUTB0
Bit 21	OUTG10

Table 8. Bit Arrangement of the APS Register (continued)

BIT OF APS REGISTERS	CORRESPONDING OUTPUTS
Bit 20	OUTG9
Bit 19	OUTG8
Bit 18	OUTG7
Bit 17	OUTG6
Bit 16	OUTG5
Bit 15	OUTG4
Bit 14	OUTG3
Bit 13	OUTG2
Bit 12	OUTG1
Bit 11	OUTG0
Bit 10	OUTR10
Bit 9	OUTR9
Bit 8	OUTR8
Bit 7	OUTR7
Bit 6	OUTR6
Bit 5	OUTR5
Bit 4	OUTR4
Bit 3	OUTR3
Bit 2	OUTR2
Bit 1	OUTR1
Bit 0	OUTR0

APS_FLAG and the APS registers are all 0 by default. After an APS check command, APS_FLAG should be 011b or 110b. Otherwise there is a failure in the APS check circuit. If the APS check result fails, the ERRn pin is pulled low, the APS_FLAG value is 110b, and the ERRn pin status stays unchanged until the fault is removed and the user executes an ERROR clear command. Figure 5 and Figure 9 show more detail.

As different LEDs have different parasitic capacitance, to make sure the APS Check function is suitable for all kinds of LEDs, the device provides two configuration bits for APS current and APS time. The APS current is selected by APS_CURRENT as shown in Table 9. The APS time is selected by APS_TIME as shown in Table 10.

Table 9. APS Current Selection

APS_CURRENT BIT	APS CURRENT
0b	20 μA
1b	40 μA

Table 10. APS Time Selection

APS_TIME BIT	ADJACENT-PIN-SHORT DETECTION TIME
0b	10 μs
1b	20 μs

8.3.4.3 IREF Short and IREF Open Detection

To protect the device from a reference-resistor short or open fault, the device integrates IREF short and open protection. In an IREF short or open fault condition, the device reports the fault and sets the output current to a default value to help improve the system safety.

By default, the ISF and IOF flags are 0. When the IREF current exceeds the fault-detection threshold, the ERRn pin is pulled down, the ISF or IOF flag is set to 1. The error flag and ERRn pin status stay unchanged until the fault is removed and there is an ERROR clear command.

Once there is an ISF or IOF failure, the output current is set to a default value, $I_{(OUT)max}$, of 10 mA, see Table 11. Once the ISF or IOF failure is removed, the output current returns back to the IREF setting value immediately.

Table 11. Criteria of ISF/IOF Judgement and Corresponding Actions

I_{IREF}	ISF	IOF	OUTPUT
$I_{IREF} \leq 10$ μA	0	1	$I_{(OUT)max}$= 10 mA
10 μA < $I_{IREF} \leq 2.3$ mA	0	0	$I_{(OUT)max} = V_{IREF} \times 40 / R_{IREF}$
$I_{IREF} > 3$ mA	1	0	$I_{(OUT)max}$ = 10 mA

8.3.4.4 Pre-Thermal Warning Flag

The HT1388 device implements a pre-thermal warning (PTW) function. Once the junction temperature exceeds the PTW threshold, the ERRn pin is pulled low, the PTW flag in error status register is set to 1, the PTW_FLAG and ERRn pin status stay unchanged until the junction temperature drops below TPTW – THYS_PTW, and there is an ERROR clear command.

8.3.4.5 Thermal Error Flag

The HT1388 device monitors junction temperature all the time. Once the junction temperature exceeds the thermal shutdown threshold, all of the constant-current outputs turn off, the ERRn pin is pulled low, the thermal error flag and ERRn pin status are set to 1 and stay unchanged until the fault is removed and there is an ERROR clear command. During this state, all the digital functions work normally, and users can read or write data through common shift registers. After the junction temperature drops below $T_{TEF} – T_{HYS\_TEF}$, the device goes back to normal operation again. Users can reset the TEF flag by sending an ERROR clear command.

8.3.4.6 Negate Bit Toggle

The HT1388 device implements a Negate Bit Toggle function to check the LOD-LSD registers, which is useful for safety-related applications.

There are NEG1 and NEG2 bits in the registers, and the values are both 0 by default. After executing the Negate Bit Toggle command, both NEG1 and NEG2 change to 1. The LOD-LSD results are reversed under this condition. If the LOD-LSD registers get stuck, the LOD-LSD results are not reversed, which means there is a fault in the LOD-LSD registers.

The LOD1-LSD1 registers only update on the 9th GCLK rising edge, and the LOD2-LSD2 registers only update on the Nth GCLK rising edge. So, after the Negate Bit Toggle command, users must wait for at least one GS counter cycle (4096 GCLKs for the 12-bit GS counter mode, 1024 GCLKs for the 10-bit GS counter mode, or 256 GCLKs for the 8-bit GS counter mode) before reading the SID registers. So if the GCLK signal is lost, it can also be detected by the negate-bit toggle function.

8.3.4.7 LOD_LSD Self-Test

The HT1388 device implements an LOD_LSD self-test function to check the LOD_LSD detection circuit to improve the system reliability. If the LOD_LSD detection circuit fails to detect the LED failure, the LOD_LSD self-test Function can identify and report the malfunction.

The LOD_LSD self-test function can be executed by sending the LOD_LSD self-test command. LOD_LSD_FLAG is 000b by default. After the LOD_LSD self-test command, if there is no fault on LOD_LSD detection circuit, and the LOD_LSD_FLAG value is 011b. If there are failures on the LOD_LSD detection circuits, the LOD_LSD_FLAG value is 110b, the ERRn pin is pulled low, and the bit values stay unchanged until the fault is removed and an ERROR clear command is executed. If the LOD_LSD_FLAG is neither 011b nor 110b, there should be something wrong in the self-test procedure.

8.3.4.8 ERRn Pin

The HT1388 device supports an active-low open-drain error output. Figure 24 shows the error pulldown block diagram. 10-bit error status information controls the error pulldown circuit directly. But LED failure can be masked by the LED_ERR_MASK bit. The LED_ERR_MASK value is 1 by default, so an LED failure is masked from the error pulldown circuit. Even if there is an LED failure, the ERRn pin is not pulled down by this LED failure. If LED_ERR_MASK is 0, the ERRn pin is pulled down by an LED failure to indicate an error scenario. Users can use an MCU interrupt to read out the fault information.

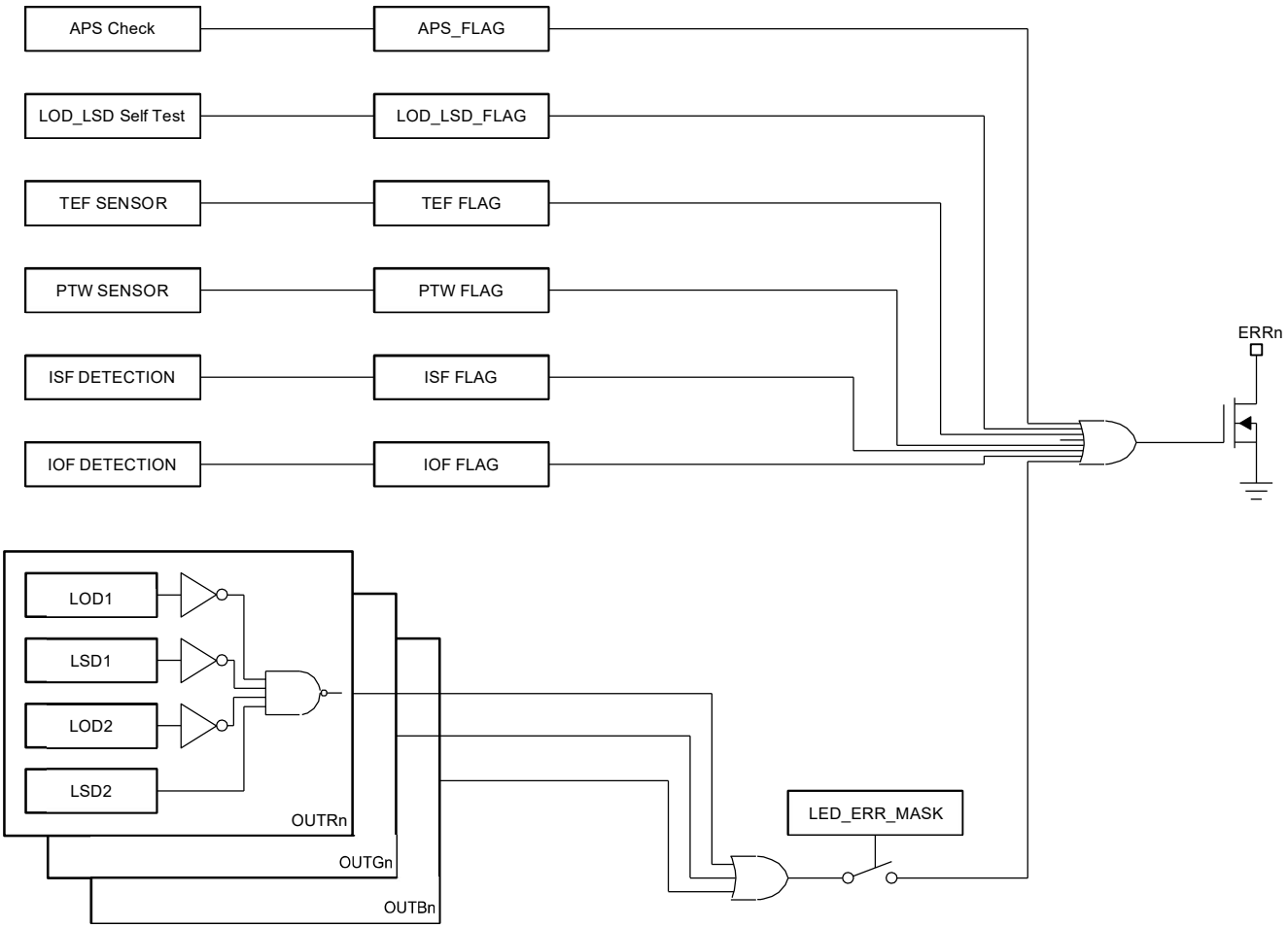


Figure 24. ERRn Pin Pulldown Scheme

8.3.4.9 ERROR Clear

This command is used to clear the error flags in the error status register and APS register. The A53h 12-bit command code indicates an ERROR clear command. After executing the ERROR clear command, the 132-bit LOD_LSD registers, 1-bit NEG1, 1-bit NEG2, 10-bit error status and 33-bit adjacent-pin-short results are loaded into the common shift register. The error status registers and APS registers are reset to 0 if the error is removed. See Figure 9 for more detail.

8.3.4.10 Global Reset

This command is used to implement a power-on reset with software input. The A5Ch 12-bit command code initiates a global reset command. After executing the global reset command, all internal registers are reset to their default values. See Figure 10 for more detail.

8.3.4.11 Slew Rate Control

To improve system EMI performance, the HT1388 device implements a programmable slew rate control for the output channels. This output slew rate is configured by the SLEW_RATE bit in the FC-BC-DC register. The SLEW_RATE bit is 0 by default, and the rising and falling time of the output is 200 ns. When the SLEW_RATE bit is 1, the rising and falling time of each output is 100 ns.

8.3.4.12 Channel Group Delay

Large surge currents may flow through the system if all 33 channels turn on simultaneously. These large current surge could induce detrimental noise and electromagnetic interference (EMI) into other circuits. The HT1388 device implements channel turn-on delay for each group to reduce the surge current. The output current sinks are grouped into six groups.

Group 1: OUTR0, -G0, -B0, OUTR6, -G6, -B6.
Group 2: OUTR1, -G1, -B1, OUTR7, -G7, -B7.
Group 3: OUTR2, -G2, -B2, OUTR8, -G8, -B8.
Group 4: OUTR3, -G3, -B3, OUTR9, -G9, -B9.
Group 5: OUTR4, -G4, -B4, OUTR10, -G10, -B10.
Group 6: OUTR5, -G5, -B5,

All group 2 channels turn on and off 50 ns later then group 1 channels, all group 3 channels turn on and off later than group 2 channels, all group 4 channels turn on and off 50 ns later than group 3 channels, all group 5 channels turn on and off 50 ns later than group 4 channels, and all group 6 channels turn on and off 50 ns later than group 5 channels. Figure 1 shows the details.

8.4 Device Functional Modes

8.4.1 Power Up

To make the device work normally, users must provide two power supplies to the HT1388 device. One is V_{CC}, 3 V–5.5 V, for device internal logic power. The other is a supply up to 5V, which is the power supply for the LED loads. To make sure the LED diagnostics feature works normally, the LED supply must connect to the SENSE pin directly.

8.4.2 Device Initialization

After device power on, users must send the error clear command and global reset command to initialize the device and make sure there are no existing faults on the circuit.

8.4.3 Fault Mode

The HT1388 has full diagnostics features. The device can detect faults and latch the faults into registers. For device faults such IREF resistor open or short, the device enters a self-protection scenario. The device reports the faults and sets the output current to a default value. For the overtemperature fault, the device turns off the output channels and latches the fault into the TEF register. Except for these two faults, for all other faults including LED faults, the device only detects and report the faults, but does not take actions to handle the faults, and the channels keep their configured status. Users must read out the faults and decide how to handle the faults.

8.4.4 Normal Operation

Users must program the device through the serial interface for normal operation. Users write to the FC-BC-DC registers to set the operation mode and output current, write to the grayscale registers to set the PWM duty cycle for each channel, and read the SID registers to get device fault information.

8.5 Programming

8.5.1 Register Write and Read

The HT1388 device is programmable via serial interface. It contains a 400-bit common shift register to shift data from SDI into the device. The register LSB connects to SDI and the MSB connects to SDO. On each SCK rising edge, the data on SDI shifts into the register LSB and all 400 data bits shift towards the MSB. The data appears on SDO when the 400-bit common shift register overflows.

The HT1388 data write command contains 400-bit data, the first 4 MSB bits from bit 399 to bit 396 are reserved and ignored. According to the following different criteria, there are three types of data write commands: FC-BC-DC write, GS data write, and special command.

- When LATCH is high at the 400th SCK rising edge, and when the 12 bits from bit 395 to bit 384 of the 400-bit data are 0, the 268 LSBs of 400-bit data shift to the function control (FC), brightness control (BC) and dot correction (DC) registers on the LATCH rising edge, as shown in Figure 2.
- When LATCH is low at the 400th SCK rising edge, the 396 LSBs of 400-bit data shifts into the grayscale (GS) configuration registers on the LATCH rising edge, as shown in Figure 1.
- When LATCH is high at the 400th SCK rising edge, and when the 12 bits from bit 395 to bit 384 of the 400-bit data match any of the twelve 12-bit command codes, the device executes the corresponding command after the LATCH rising edge, as shown in Special Command Function.

When the device powers on, the default value of the 400-bit common shift register is 0.

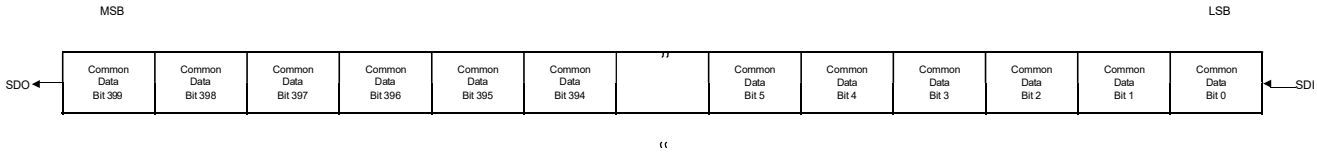


Figure 25. HT1388 Common Register

8.5.1.1 FC-BC-DC Write

The device latches the 268 LSBs of data in the 400-bit common shift register into the FC-BC-DC registers at the rising edge of the latch signal when the 12 bits from bit 395 to bit 384 of the 400-bit data are 0.

When the device is powered on, the FC-BC-DC data latch is reset to all 0s except for the LED_ERR_MASK bit which is 1. Therefore, data must be written to the 400-bit common shift register and latched into the FC-BC-DC registers before turning on the constant-current outputs. It is better to keep BLANK low to prevent the outputs from turning on.

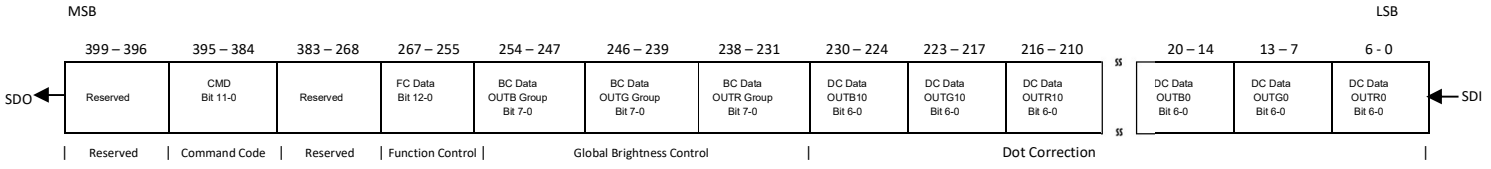


Figure 26. FC-BC-DC Register

8.5.1.1.1 FC Data Write

The FC data is 13 bits in length, located from bit 267 to bit 255. See Table 12 for the detailed description. The default value for all FC data is 0, except for the LED_ERR_MASK bit which is 1.

Table 12. Function-Control Data-Bit Assignment

BIT	NAME	DESCRIPTION
267	LED_ERR_MASK	LOD-LSD failure or PWM error information mask bit 0b = Any LOD-LSD failure or PWM error pulls down the ERRn pin 1b = LOD-LSD failure or PWM error is masked from affecting the ERRn pin
266	SLEW_RATE	Turnon and turnoff speed configuration bit 0b = 200 ns rising and falling time. 1b = 100 ns rising and falling time.
265	LOD_VOLATGE	LED open-detection (LOD) threshold 0b = LOD threshold is 0.3 V 1b = LOD threshold is 0.5 V
264	LSD_VOLTAGE	LED short-detection (LSD) threshold 0b = LSD threshold is V_{SENSE} – 0.3 V 1b = LSD threshold is V_{SENSE} – 0.7 V
265	APS_CURRENT	Adjacent-pin short-detection sink current 0b = 20-µA APS current 1b = 40-µA APS current
262	APS_TIME	Adjacent-pin short-detection time 0b = 10 µs APS detection time 1b = 20 µs APS detection time
261–260	GS_MODE	Grayscale-counter mode selection. 00/01b = 12-bit mode 10 = 10-bit mode 11 = 8-bit mode
259	TIMING_RESET	Display-timing reset mode 0b = Disabled 1b = Enabled
258	AUTO_REPEAT	Auto-display repeat mode 0b = Disabled 1b = Enabled
257	DC_RANGE_B	Dot-correction adjustment range for the BLUE color output 0b = Lower range 0%–66.7% 1b = Higher range
256	DC_RANGE_G	Dot-correction adjustment range for the GREEN color output 0b = Lower range 0%–66.7% 1b = Higher range
255	DC_RANGE_R	Dot–correction adjustment range for the RED color output 0b = Lower range 0%–66.7% 1b = Higher range

The grayscale counter has 12-bit, 10-bit and 8-bit configurations. Bits 261–260 in the FC register configure the grayscale counter mode.

Table 13. GS Counter Mode Table

GRAYSCALE COUNTER MODE (GS_MODE)		FUNCTION MODE
BIT 261	BIT 260	
0	Don't care	12-bit counter mode
1	0	10-bit counter mode, the lowest 10 bits of the 12-bit GS data are valid
1	1	8-bit counter mode, the lowest 8 bits of the 12-bit GS data are valid

8.5.1.1.2 BC Data Write

The BC data is 24 bits length which locates from bit 254 to bit 231.The data of the BC data latch are used to adjust the constant-current values for eleven channel constant-current drivers of each color group. The current can be adjusted from 0% to 100% of each output current adjusted by brightness control with 8-bit resolution.

Table 14. Brightness Control Data Bit Assignments

BITS	BRIGHTNESS CONTROL DATA
254–247	OUTB0-OUTB7 group
246–239	OUTG0-OUTG7 group
238–231	OUTR0-OUTR7 group

8.5.1.1.3 DC Data Write

The DC data is 231 bits in length, located from bit 230 to bit 0. The HT1388 device can adjust the output current of each channel using the DC function. The DC function has two adjustment ranges with 7-bit resolution. Table 15 shows the DC data assignments in the DC registers. The high adjustment range DC can adjust output current from 33.3% to 100% of $I_{(OUT)max}$. The low adjustment range DC can adjust output current from 0% to 66.7% of $I_{(OUT)max}$. The range control is in bits 257–255 in the function control data latch select the high or low adjustment. Bit 257 controls the OUTB DC range. Bit 256 controls the OUTG DC range, Bit 255 controls the OUTR DC range. For details, see Table 12

Table 15. DC Data Assignments

BITS	DATA	BITS	DATA
		118–112	OUTG5
230-224	OUTB10	111–105	OUTR5
223-217	OUTG10	104–98	OUTB4
216-210	OUTR10	97–91	OUTG4
209-203	OUTB9	90–84	OUTR4
202-196	OUTG9	83–77	OUTB3
195-189	OUTR9	76–70	OUTG3
188-182	OUTB8	69–63	OUTR3
181-175	OUTG8	62–56	OUTB2

Table 15. DC Data Assignments (continued)

BITS	DATA	BITS	DATA
174-168	OUTR8	55–49	OUTG2
167–161	OUTB7	48–42	OUTR2
160–154	OUTG7	41–35	OUTB1
153–147	OUTR7	34–28	OUTG1
146–140	OUTB6	27–21	OUTR1
139–133	OUTG6	20–14	OUTB0
132–126	OUTR6	13–7	OUTG0
125–119	OUTB5	6–0	OUTR0

Table 16. Output Current vs DC (High DC Range)

DC DATA (BIN)	DC DATA (DEC)	DC DATA (HEX)	BC DATA (HEX)	CURRENT RATIO (%)	CURRENT ($I_{(OUT)max}$ = 30 mA)	CURRENT ($I_{(OUT)max}$ = 2 mA)
000 0000	0	00	FF	33.3	10.00	0.67
000 0001	1	01	FF	33.9	10.16	0.68
000 0010	2	02	FF	34.4	10.31	0.69
...	...	...	...	...	...	...
111 1101	125	7D	FF	99	29.69	1.98
111 1110	126	7E	FF	99.5	29.84	1.99
111 1111	127	7F	FF	100	30.00	2

Table 17. Output Current vs DC (Low DC Range)

DC DATA (BIN)	DC DATA (DEC)	DC DATA (HEX)	BC DATA (HEX)	CURRENT RATIO (%)	CURRENT ($I_{(OUT)max}$ = 30 mA)	CURRENT ($I_{(OUT)max}$ = 2 mA)
000 0000	0	00	FF	0	0.00	0
000 0001	1	01	FF	0.5	0.16	0.01
000 0010	2	02	FF	1.0	0.31	0.02
...	...	...	...	...	...	...
111 1101	125	7D	FF	65.6	19.69	1.31
111 1110	126	7E	FF	66.1	19.84	1.32
111 1111	127	7F	FF	66.7	20.00	1.33

Table 18. Output Current vs BC (High DC Range)

BC DATA (BIN)	BC DATA (DEC)	BC DATA (HEX)	DC DATA (HEX)	CURRENT RATIO (%)	CURRENT ($I_{(OUT)max}$ = 30 mA)	CURRENT ($I_{(OUT)max}$ = 2 mA)
0000 0000	0	00	7F	0	0.00	0
0000 0001	1	01	7F	0.4	0.12	0.01
0000 0010	2	02	7F	0.8	0.24	0.02
...	...	...	...	...	...	...
1111 1101	253	FD	7F	99.2	29.76	1.98
1111 1110	254	FE	7F	99.6	29.88	1.99
1111 1111	255	FF	7F	100	30.00	2

8.5.1.2 Grayscale Data Write

The grayscale data, which is 396 bits long, contains a 12-bit grayscale value for each output. The grayscale value sets the channel turn-on time.Figure 27 shows the GS register configuration. Figure 1 is the GS write timing diagram. The 396 LSBs Data is latched from the 400-Bit common shift register into the GS data latch at the rising edge of the LATCH pin. When data is latched into the GS registers, the new data is immediately available on the constant- current outputs. If data are latched with BLANK high, the outputs may turn on or off unexpectedly. So users should update the GS data when BLANK is low.

The 12-bit GS function has 4096 brightness steps, from 0% to 99.97% brightness. The GS function is controlled by a 12-bit GS counter. The GS counter increments on each rising edge of the grayscale reference clock, GCLK. The falling edge of BLANK resets the GS counter value to 0. The GS counter value stays 0 while BLANK is low, even if there is a GCLK input. Pulling BLANK high enables the 12-bit GS counter. The first rising edge of a GS clock after BLANK goes high increments the GS counter by 1 and turns on the outputs. Each additional rising edge increases the GS counter by 1. The GS counter monitors the number of clock pulses on the GCLK pin. The output stays on while the counter value is less than or equal to the GS setting value. The output turns off at the rising edge of the GS counter value when the counter is higher than the GS setting value. Table 20 is the on-time duty cycle of each GS data bit when 12-bit GS counter mode selected.

When the device is powered up, the 400-bit common shift register and GS data latch are reset to 0.

Equation 4 describes each output on time.

$$t_{on} = t_{GCLK} \times GS \quad (4)$$

where

- t_{GCLK} is the GS clock period
- GS is the programmed grayscale value for each output

Equation 5 shows the duty cycle calculation equation.

$$Dutycycle = \frac{GS}{4096} \quad (5)$$

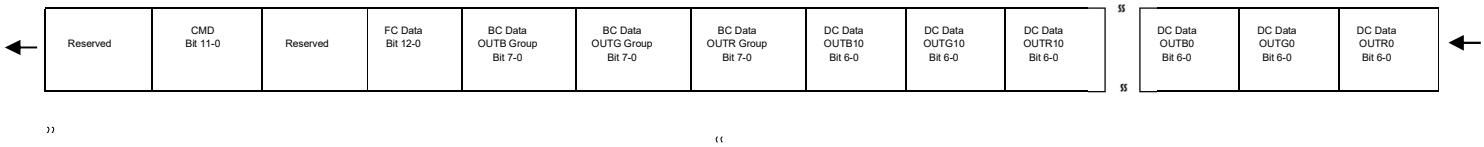


Figure 27. HT1388 Grayscale Register

Once the GS data is latched into the GS registers at the rising edge of the LATCH signal, the FC-BC-DC data latch shifts into the lowest 268 bits of the common shift register. So, the FC-BC-DC data can be read out from SDO in GS write. This FC-BC-DC read function can also be realized by the read FC-BC-DC command, see FC-BC-DC Read for the timing diagram.

Table 19. Grayscale Data Bit Assignments

BITS	DATA
395-384	OUTB10
383-372	OUTG10
371-360	OUTR10
359-348	OUTB9
347-336	OUTG9

335-324	OUTR9
323-312	OUTB8
311-300	OUTG8
299-288	OUTR8
287-276	OUTB7
275-264	OUTG7
263-252	OUTR7
251-240	OUTB6
239-228	OUTG6
227-216	OUTR6
215-204	OUTB5
203-192	OUTG5
191-180	OUTR5
179-168	OUTB4
167-156	OUTG4
155-144	OUTR4
143-132	OUTB3
131-120	OUTG3
119-108	OUTR3
107-96	OUTB2
95-84	OUTG2
83-72	OUTR2
71-60	OUTB1
59-48	OUTG1
47-36	OUTR1
35-24	OUTB0
23-12	OUTG0
11-0	OUTR0

Table 19. Grayscale Data Bit Assignments (continued)

Table 20. GS Data vs Output On Time

GS DATA (BINARY)	GS DATA (DECIMAL)	GS DATA (HEX)	DUTY CYCLE (%)	ON-TIME BASED ON 33-MHz GS CLOCK (ns)
0000 0000 0000	0	000	0	0
0000 0000 0001	1	001	0.02	30
0000 0000 0010	2	002	0.05	61
...	...	...	...	...
0111 1111 1111	2047	7FF	49.97	62 030
1000 0000 0000	2048	800	50.00	62 061
1000 0000 0001	2049	801	50.02	62 091
...	...	...	...	...
1111 1111 1101	4093	FFD	99.93	124 030
1111 1111 1110	4094	FFE	99.95	124 061
1111 1111 1111	4095	FFF	99.98	124 091

7.5.1.3 Special Command Function

There are twelve special command codes defined in the HT1388 device, shown in Table 21. To input the command, the level of LATCH at the last SCK before the LATCH rising edge must be high, and the highest 12 bits should be one of the listed 12 command codes. In this condition, the device ignores other bits and no data are latched into FC-BC-DC registers. Normally users can write other bits to 0 in the special command. The corresponding command function executes after the rising edge of the LATCH signal.

If no special command code is identified, the command is a NULL command and no special command is executed. The command is the same as the FC-BC-DC write function.

Table 21. Special Command Codes

COMMAND	COMMAND CODE	FUNCTION
Lookahead	A5Dh (1010 0101 1101b)	Sets lookahead pin value to 1, to preview the target trimming value
Zap	A5Eh (1010 0101 1110b)	Sends a ZAP pulse action to burn out the fuse
Sleep	A58h (1010 0101 1000b)	Enters Sleep mode. When sleep mode is entered, all analog peripherals will be turn off while the value set at the FC-BC-DC and GS Data registers would be retained.
Wakeup	A5Ah (1010 0101 1010b)	Exits Sleep mode. When exiting sleep mode, the logic will gate the signals to the analog block until the analog_rdy signal is high.
GS read	5AFh (0101 1010 1111b)	Load GS data into common register.
SID read	5A3h (0101 1010 0011b)	Load SID data into common register.
FC-BC-DC read	5ACh (0101 1010 1100b)	Load FC-BC-DC data into common register. This reading function can also be achieved by GS data write.
APS check	53Ah (0101 0011 1010b)	Adjacent pin short detection, APS test starts at the rising edge of Latch signal, then set APS register(24bits) and APS_Flag in SID register according to the test result. Keep all channels off during this test.
LOD_LSD self-test	535h (0101 0011 0101b)	LOD-LSD detector circuit self test and set LOD_LSD_FLAG in SID register according to the test result.
Negate bit toggle	55Ah (0101 0101 1010b)	Toggle Negate Bit. When Negate Bit = 0, the 48 bits LOD-LSD detector output data will be latched into LOD1-LSD1 and LOD2-LSD2 register without invert. When Negate Bit =1, the 48 bits LOD-LSD detector output data will invert, and latch into LOD1-LSD1 and LOD2-LSD2 register.

ERROR clear	A53h (1010 0101 0011b)	Load SID data into common register, and then reset the Error status register and APS register to 0.
GLOBAL reset	A5Ch (1010 0101 1100b)	All internal registers are reset. The command has the same function as power on reset.
NULL	Different from any of the above commands	The same function as FC-BC-DC write.

8.5.1.3.1 GS Read

The GS read command loads 396-bits of GS data into the lowest 396 bits of the common shift register. By applying 400 SCK clocks, the GS data shifts out from the SDO pin. For details, see Figure 3.

8.5.1.3.2 FC-BC-DC Read

There are two ways to read the FC-BC-DC data latch.

One way is latching data into the GS data latch. After the GS write finishes, the FC-BC-DC data latches into the lowest 268 bits of the common shift register.

Another way is using the FC-BC-DC read command. After the FC-BC-DC read command finishes, the FC-BC-DC data latches into the lowest 268 bits of the common shift register.

By applying 400 SCK clocks, the FC-BC-DC data shifts out from the SDO pin. For details, see Figure 8.

8.5.1.3.3 Status Information Data Read

Status information data (SID) is 177 bits long and contains device status information and LED fault information. Table 22 describes the bit mapping when SID data loads into the common shift register.

Bits 176–111 are the LED-open information for the output channels, bits 65–0 are the LED-short information for the output channels, bits 110-78 are the adjacent-pin-short information for the output channels, bits 77–68 are the error status registers, bits 67–66 are the negate bits.

After power on, all error status registers are set to 0. If any one of the error-status-register flags (bits 215–206) asserts, the registers latch the faults until a reset error command is executed to clear the faults. But the LOD_LSD data continues to update every PWM cycle.

Table 22. SID Register

BITS OF COMMON SHIFT REGISTER	DESCRIPTION
176-166	LOD2 data for OUTB10-OUTB0
165-155	LOD2 data for OUTG10-OUTG0
154-144	LOD2 data for OUTR10-OUTR0
143-133	LOD1 data for OUTB10-OUTB0
132-122	LOD1 data for OUTG10-OUTG0
121-111	LOD1 data for OUTR10-OUTR0
110-100	APS status data for OUTB10-OUTB0
99-89	APS status data for OUTG10-OUTG0
88-78	APS status data for OUTR10-OUTR0
77	Thermal error flag.
76	Pre-thermal warning flag. 0b=No pre-thermal warning, 1b=Pre-thermal threshold triggered.
75-73	APS test flag fault. 011b: Pass, 110b: Fail
72	IREF Short fault flag. 0b=IREF not shorted, 1b=IREF short detected
71	IREF Open fault flag. 0b=IREF not open, 1b=IREF open detected
70-68	LOD_LSD self-test flag. 011b: Pass, 110b: Fail

67	Negate bit for LOD1-LSD1 register
66	Negate bit for LOD2-LSD2 register
65-55	LSD2 data for OUTB10-OUTB0
54-44	LSD2 data for OUTG10-OUTG0
43-33	LSD2 data for OUTR10-OUTR0
32-22	LSD1 data for OUTB10-OUTB0
21-11	LSD1 data for OUTG10-OUTG0
10-0	LSD1 data for OUTR10-OUTR0

8.6 Register Maps

The HT1388 register map includes three sections: GS registers, FC_BC_DC registers, and SID registers. Users can write to the GS registers and FC_BC_DC registers through the serial interface. Status Information can be read out though the serial interface.

8.6.1 GRAYSCALE Registers

Table 23 lists the memory-mapped registers for the GRAYSCALE. All register offset addresses not listed in Table 23 should be considered as reserved locations and the register contents should not be modified.

Grayscale Register

Table 23. GRAYSCALE Registers

Offset	Acronym	Register Name	Section
0h	OUTn_GS	Output Grayscale Register	Go

Complex bit access types are encoded to fit into small table cells. Table 24 shows the codes that are used for access types in this section.

Table 24. GRAYSCALE Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 OUTn_GS Register (Offset = 0h)

OUTn_GS is shown in Figure 28 and described in Table 25.

Return to Summary Table.

OUTn Grayscale Register

Figure 28. OUTn_GS Register

								399	398	397	396
								RESERVED			
								R/W-0h			
395	394	393	392	391	390	389	388	387	386	385	384
OUTB10_GS											
R/W-0h											
383	382	381	380	379	378	377	376	375	374	373	372
OUTG10_GS											
R/W-0h											
371	370	369	368	367	366	365	364	363	362	361	360
OUTR10_GS											
R/W-0h											
359	358	357	356	355	354	353	352	351	350	349	348

OUTB9_GS											
R/W-0h											
347	346	345	344	343	342	341	340	339	338	337	336
OUTG9_GS											
R/W-0h											
335	334	333	332	331	330	329	328	327	326	325	324
OUTR9_GS											
R/W-0h											
323	322	321	320	319	318	317	316	315	314	313	312
OUTB8_GS											
R/W-0h											
311	310	309	308	307	306	305	304	303	302	301	300
OUTG8_GS											
R/W-0h											
299	298	297	296	295	294	293	292	291	290	289	288
OUTR8_GS											
R/W-0h											
287	286	285	284	283	282	281	280	279	278	277	276
OUTB7_GS											
R/W-0h											
275	274	273	272	271	270	269	268	267	266	265	264
OUTG7_GS											
R/W-0h											
263	262	261	260	259	258	257	256	255	254	253	252
OUTR7_GS											
R/W-0h											
251	250	249	248	247	246	245	244	243	242	241	240
OUTB6_GS											
R/W-0h											
239	238	237	236	235	234	233	232	231	230	229	228
OUTG6_GS											
R/W-0h											
227	226	225	224	223	222	221	220	219	218	217	216
OUTR6_GS											
R/W-0h											

215	214	213	212	211	210	209	208	207	206	205	204
OUTB5_GS											
R/W-0h											
203	202	201	200	199	198	197	196	195	194	193	192
OUTG5_GS											
R/W-0h											
191	190	189	188	187	186	185	184	183	182	181	180
OUTR5_GS											
R/W-0h											
179	178	177	176	175	174	173	172	171	170	169	168
OUTB4_GS											
R/W-0h											
167	166	165	164	163	162	161	160	159	158	157	156
OUTG4_GS											
R/W-0h											
155	154	153	152	151	150	149	148	147	146	145	144
OUTR4_GS											
R/W-0h											
143	142	141	140	139	138	137	136	135	134	133	132
OUTB3_GS											
R/W-0h											
131	130	129	128	127	126	125	124	123	122	121	120
OUTG3_GS											
R/W-0h											
119	118	117	116	115	114	113	112	111	110	109	108
OUTR3_GS											
R/W-0h											
107	106	105	104	103	102	101	100	99	98	97	96
OUTB2_GS											
R/W-0h											
95	94	93	92	91	90	89	88	87	86	85	84
OUTG2_GS											
R/W-0h											
83	82	81	80	79	78	77	76	75	74	73	72
OUTR2_GS											
R/W-0h											
71	70	69	68	67	66	65	64	63	62	61	60
OUTB1_GS											
R/W-0h											
59	58	57	56	55	54	53	52	51	50	49	48
OUTG1_GS											
R/W-0h											
47	46	45	44	43	42	41	40	39	38	37	36
OUTR1_GS											
R/W-0h											

35	34	33	32	31	30	29	28	27	26	25	24
OUTB0_GS											
R/W-0h											
23	22	21	20	19	18	17	16	15	14	13	12
OUTG0_GS											
R/W-0h											
11	10	9	8	7	6	5	4	3	2	1	0
OUTR0_GS											
R/W-0h											

Table 25. OUTn_GS Register Field Descriptions

Bit	Field	Type	Default	Description
395–384	OUTB10_GS[11:0]	R/W	0h	Grayscale register for OUTB10
383–372	OUTG10_GS[11:0]	R/W	0h	Grayscale register for OUTG10
371–360	OUTR10_GS[11:0]	R/W	0h	Grayscale register for OUTR10
359–348	OUTB9_GS[11:0]	R/W	0h	Grayscale register for OUTB9
347–336	OUTG9_GS[11:0]	R/W	0h	Grayscale register for OUTG9
335–324	OUTR9_GS[11:0]	R/W	0h	Grayscale register for OUTR9
323–312	OUTB8_GS[11:0]	R/W	0h	Grayscale register for OUTB8
311–300	OUTG8_GS[11:0]	R/W	0h	Grayscale register for OUTG8
299–288	OUTR8_GS[11:0]	R/W	0h	Grayscale register for OUTR8
287–276	OUTB7_GS[11:0]	R/W	0h	Grayscale register for OUTB7
275–264	OUTG7_GS[11:0]	R/W	0h	Grayscale register for OUTG7
263–252	OUTR7_GS[11:0]	R/W	0h	Grayscale register for OUTR7
251–240	OUTB6_GS[11:0]	R/W	0h	Grayscale register for OUTB6
239–228	OUTG6_GS[11:0]	R/W	0h	Grayscale register for OUTG6
227–216	OUTR6_GS[11:0]	R/W	0h	Grayscale register for OUTR6
215–204	OUTB5_GS[11:0]	R/W	0h	Grayscale register for OUTB5
203–192	OUTG5_GS[11:0]	R/W	0h	Grayscale register for OUTG5
191–180	OUTR5_GS[11:0]	R/W	0h	Grayscale register for OUTR5
179–168	OUTB4_GS[11:0]	R/W	0h	Grayscale register for OUTB4
167–156	OUTG4_GS[11:0]	R/W	0h	Grayscale register for OUTG4
155–144	OUTR4_GS[11:0]	R/W	0h	Grayscale register for OUTR4
143–132	OUTB3_GS[11:0]	R/W	0h	Grayscale register for OUTB3
131–120	OUTG3_GS[11:0]	R/W	0h	Grayscale register for OUTG3
119–108	OUTR3_GS[11:0]	R/W	0h	Grayscale register for OUTR3
107–96	OUTB2_GS[11:0]	R/W	0h	Grayscale register for OUTB2
95–84	OUTG2_GS[11:0]	R/W	0h	Grayscale register for OUTG2
83–72	OUTR2_GS[11:0]	R/W	0h	Grayscale register for OUTR2

71–60	OUTB1_GS[11:0]	R/W	0h	Grayscale register for OUTB1
59–48	OUTG1_GS[11:0]	R/W	0h	Grayscale register for OUTG1
47–36	OUTR1_GS[11:0]	R/W	0h	Grayscale register for OUTR1
35–24	OUTB0_GS[11:0]	R/W	0h	Grayscale register for OUTB0
23–12	OUTG0_GS[11:0]	R/W	0h	Grayscale register for OUTG0
11–0	OUTR0_GS[11:0]	R/W	0h	Grayscale register for OUTR0

8.6.2 FC-BC-DC Registers

Table 26 lists the memory-mapped registers for the FC-BC-DC. All register offset addresses not listed in Table 26 should be considered as reserved locations and the register contents should not be modified.

FC-BC-DC Register

Table 26. FC-BC-DC Registers

Offset	Acronym	Register Name	Section
1h	FC-BC-DC	FC-BC-DC Register	Go

Complex bit access types are encoded to fit into small table cells. Table 27 shows the codes that are used for access types in this section.

Table 27. FC-BC-DC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.1 FC-BC-DC Register (Offset = 1h)

FC-BC-DC is shown in Figure 29 and described in Table 28.

Return to Summary Table.

FC-BC-DC Register

Figure 29. FC-BC-DC Register

												399	398	397	396
												RESERVED			
												R/W-0h			
395	394	393	392	391	390	389	388	387	386	385	384	383	382	381	380
CMD												RESERVED			
R/W-0h												R/W-0h			
379	378	377	376	375	374	373	372	371	370	369	368	367	366	365	364
RESERVED															
R/W-0h															
363	362	361	360	359	358	357	356	355	354	353	352	351	350	349	348
RESERVED															
R/W-0h															
347	346	345	344	343	342	341	340	339	338	337	336	335	334	333	332
RESERVED															
R/W-0h															
331	330	329	328	327	326	325	324	323	322	321	320	319	318	317	316
RESERVED															
R/W-0h															
315	314	313	312	311	310	309	308	307	306	305	304	303	302	301	300
RESERVED															
R/W-0h															
299	298	297	296	295	294	293	292	291	290	289	288	287	286	285	284
RESERVED															
R/W-0h															
283	282	281	280	279	278	277	276	275	274	273	272	271	270	269	268
RESERVED															
R/W-0h															
267	266	265	264	263	262	261	260	259	258	257	256	255	254	253	252
LED_ERR_MASK	SLEW_RATE	LOD_VOLTAGE	LSD_VOLTAGE	APS_CURRENT	APS_TIME	GS_MODE		TIMING_RESET	AUTO_REPEAT	DC_RANGE_B	DC_RANGE_G	DC_RANGE_R	OUTB_BC		
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		
251	250	249	248	247	246	245	244	243	242	241	240	239	238	237	236
OUTB_BC					OUTG_BC								OUTR_BC		
R/W-0h					R/W-0h								R/W-0h		
235	234	233	232	231	230	229	228	227	226	225	224	223	222	221	220
OUTR_BC					OUTB10_DC							OUTG10_DC			
R/W-0h					R/W-0h							R/W-0h			
219	218	217	216	215	214	213	212	211	210	209	208	207	206	205	204
OUTG10_DC			OUTR10_DC							OUTB9_DC					→
R/W-0h			R/W-0h							R/W-0h					→
203	202	201	200	199	198	197	196	195	194	193	192	191	190	189	188
←	OUTG9_DC							OUTR9_DC							→
←	R/W-0h							R/W-0h							→

187	186	185	184	183	182	181	180	179	178	177	176	175	174	173	172
OUTB8_DC						OUTG8_DC							OUTR8_DC		
R/W-0h						R/W-0h							R/W-0h		

171	170	169	168	167	166	165	164	163	162	161	160	159	158	157	156
OUTR8_DC				OUTB7_DC							OUTG7_DC				
R/W-0h				R/W-0h							R/W-0h				

155	154	153	152	151	150	149	148	147	146	145	144	143	142	141	140
OUTG7_DC		OUTR7_DC							OUTB6_DC						
R/W-0h		R/W-0h							R/W-0h						

139	138	137	136	135	134	133	132	131	130	129	128	127	126	125	124
OUTG6_DC							OUTR6_DC							OUTB5_DC	
R/W-0h							R/W-0h							R/W-0h	

123	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108
OUTB5_DC						OUTG5_DC							OUTR5_DC		
R/W-0h						R/W-0h							R/W-0h		

107	106	105	104	103	102	101	100	99	98	97	96	95	94	93	92
OUTR5_DC				OUTB4_DC						OUTG4_DC					→
R/W-0h				R/W-0h						R/W-0h					→

91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76
←		OUTR4_DC						OUTB3_DC							→
←		R/W-0h						R/W-0h							→

75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60
←	OUTG3_DC					OUTR3_DC							OUTB2_DC		
←	R/W-0h					R/W-0h							R/W-0h		

59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44
OUTB2_DC				OUTG2_DC							OUTR2_DC				
R/W-0h				R/W-0h							R/W-0h				

43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28
OUTR2_DC		OUTB1_DC							OUTG1_DC						
R/W-0h		R/W-0h							R/W-0h						

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12
OUTB1_DC							OUTB0_DC							OUTG0_DC	
R/W-0h							R/W-0h							R/W-0h	

11	10	9	8	7	6	5	4	3	2	1	0				
OUTG0_DC				OUTR0_DC											
R/W-0h				R/W-0h											

Table 28. FC-BC-DC Register Field Descriptions

Bit	Field	Type	Default	Description
399–396	RESERVED	R/W	0h	Reserved
395 – 384	CMD[11:0]	R/W	0h	Command function 25Ch = Global reset 535h = LOD_LSD self-test 53Ah = APS check 55Ah = NEG-BIT toggle 5A3h = SID read 5ACh = FC_BC_DC read 5AFh = GS read A53h = ERROR clear A58h = Sleep A5Ah = Wakeup A5Dh = Lookahead A5Eh = Zap
383–268	RESERVED	R/W	0h	Reserved
267	LED_ERR_MASK	R/W	1h	LED error mask 0h = Unmask LED error 1h = Mask LED error
266	SLEW_RATE	R/W	0h	Output slew-rate time 0h = 100 ns 1h = 200 ns
265	LOD_VOLTAGE	R/W	0h	LED open-detection voltage 0h = 0.3 V 1h = 0.5 V
264	LSD_VOLTAGE	R/W	0h	LED short-detection voltage 0h = VSENSE - 0.3 V 1h = VSENSE - 0.7 V
263	APS_CURRENT	R/W	0h	Adjacent-pin short-detection sink current 0h = 20 µA 1h = 40 µA
262	APS_TIME	R/W	0h	Adjacent-pin short-detection time 0h = 10 µs 1h = 20 µs

261–260	GS_MODE[1:0]	R/W	0h	Grayscale counter mode 0h or 1h = 12-bit counter mode 2h = 10-bit counter mode 3h = 8-bit counter mode
259	TIMING_RESET	R/W	0h	Display timing reset 0h = Disabled 1h = Enabled
258	AUTO_REPEAT	R/W	0h	Auto repeat 0h = Disabled 1h = Enabled
257	DC_RANGE_B	R/W	0h	Dot correction range for OUTB group 0h = Low range 1h = High range
256	DC_RANGE_G	R/W	0h	Dot correction range for OUTG group 0h = Low range 1h = High range
255	DC_RANGE_R	R/W	0h	Dot correction range for OUTR group 0h = Low range 1h = High range
254–247	OUTB_BC[7:0]	R/W	0h	Brightness control for OUTB group
246–239	OUTG_BC[7:0]	R/W	0h	Brightness control for OUTG group
238–231	OUTR_BC[7:0]	R/W	0h	Brightness control for OUTR group
230:224	OUTB10_DC[6:0]	R/W	0h	Dot correction for OUTB10
223:217	OUTG10_DC[6:0]	R/W	0h	Dot correction for OUTG10
216:210	OUTR10_DC[6:0]	R/W	0h	Dot correction for OUTR10
209:203	OUTB9_DC[6:0]	R/W	0h	Dot correction for OUTB9
202:196	OUTG9_DC[6:0]	R/W	0h	Dot correction for OUTG9
195:189	OUTR9_DC[6:0]	R/W	0h	Dot correction for OUTR9
188:182	OUTB8_DC[6:0]	R/W	0h	Dot correction for OUTB8
181:175	OUTG8_DC[6:0]	R/W	0h	Dot correction for OUTG8
174:168	OUTR8_DC[6:0]	R/W	0h	Dot correction for OUTR8
167–161	OUTB7_DC[6:0]	R/W	0h	Dot correction for OUTB7
160–154	OUTG7_DC[6:0]	R/W	0h	Dot correction for OUTG7
153–147	OUTR7_DC[6:0]	R/W	0h	Dot correction for OUTR7
146–140	OUTB6_DC[6:0]	R/W	0h	Dot correction for OUTB6
139–133	OUTG6_DC[6:0]	R/W	0h	Dot correction for OUTG6

132–126	OUTR6_DC[6:0]	R/W	0h	Dot correction for OUTR6
125–119	OUTB5_DC[6:0]	R/W	0h	Dot correction for OUTG5
118–112	OUTG5_DC[6:0]	R/W	0h	Dot correction for OUTB5
111–105	OUTR5_DC[6:0]	R/W	0h	Dot correction for OUTR5
104–98	OUTB4_DC[6:0]	R/W	0h	Dot correction for OUTB4
97–91	OUTG4_DC[6:0]	R/W	0h	Dot correction for OUTG4
90–84	OUTR4_DC[6:0]	R/W	0h	Dot correction for OUTR4
83–77	OUTB3_DC[6:0]	R/W	0h	Dot correction for OUTB3
76–70	OUTG3_DC[6:0]	R/W	0h	Dot correction for OUTG3
69–63	OUTR3_DC[6:0]	R/W	0h	Dot correction for OUTR3
62–56	OUTB2_DC[6:0]	R/W	0h	Dot correction for OUTB2
55–49	OUTG2_DC[6:0]	R/W	0h	Dot correction for OUTG2
48–42	OUTR2_DC[6:0]	R/W	0h	Dot correction for OUTR2
41–35	OUTB1_DC[6:0]	R/W	0h	Dot correction for OUTB1
34–28	OUTG1_DC[6:0]	R/W	0h	Dot correction for OUTG1
27–21	OUTR1_DC[6:0]	R/W	0h	Dot correction for OUTR1
20–14	OUTB0_DC[6:0]	R/W	0h	Dot correction for OUTB0
13–7	OUTG0_DC[6:0]	R/W	0h	Dot correction for OUTG0
6–0	OUTR0_DC[6:0]	R/W	0h	Dot correction for OUTR0

8.6.3 SID Registers

Table 29 lists the memory-mapped registers for the SID. All register offset addresses not listed in Table 29 should be considered as reserved locations and the register contents should not be modified.

SID Register

Table 29. SID Registers

Offset	Acronym	Register Name	Section
2h	SID	SID Register	Go

Complex bit access types are encoded to fit into small table cells. Table 30 shows the codes that are used for access types in this section.

Table 30. SID Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.6.3.1 SID Register (Offset = 2h)

SID is shown in Figure 30 and described in Table 31.

Return to Summary Table.

Status information data

Figure 30. SID Register

399	398	397	396	395	394	393	392	391	390	389	388	387	386	385	384
RESERVED															
R-0h															
383	382	381	380	379	378	377	376	375	374	373	372	371	370	369	368
RESERVED															
R-0h															
367	366	365	364	363	362	361	360	359	358	357	356	355	354	353	352
RESERVED															
R-0h															
351	350	349	348	347	346	345	344	343	342	341	340	339	338	337	336
RESERVED															
R-0h															
335	334	333	332	331	330	329	328	327	326	325	324	323	322	321	320
RESERVED															
R-0h															
319	318	317	316	315	314	313	312	311	310	309	308	307	306	305	304
RESERVED															
R-0h															
287	286	285	284	283	282	281	280	279	278	277	276	275	274	273	272
RESERVED															
R-0h															
271	270	269	268	267	266	265	264	263	262	261	260	259	258	257	256
RESERVED															
R -0h															

255	254	253	252	251	250	249	248	247	246	245	244	243	242	241	240
RESERVED															
R/-0h															
239	238	237	236	235	234	233	232	231	230	229	228	227	226	225	224
RESERVED															
R-0h															
223	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208
RESERVED															
R-0h															
207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192
RESERVED															
R-0h															
191	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176
RESERVED															→
R-0h															→
175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160
OUTB_LOD2										OUTG_LOD2					
R-0h										R-0h					
159	158	157	156	155	154	153	152	151	150	149	148	147	146	145	144
OUTG_LOD2						OUTR_LOD2									
R-0h						R-0h									
143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128
OUTB_LOD1										OUTG_LOD1					
R-0h										R-0h					
127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
OUTG_LOD1						OUTR_LOD1									
R-0h						R-0h									
111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
←	OUTB_APS											OUTG_APS			
←	R-0h											R-0h			
95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
OUTG_APS							OUTR_APS								
R-0h							R-0h								
79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
OUTR_APS	TEF	PTW	APS_FLAG				ISF	IOF	LOD_LSD_FLAG			NEG1	NEG0	OUTB_LSD2	
R-0h	R-0h	R-0h	R-0h				R-0h	R-0h	R-0h			R-0h	R-0h	R-0h	
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
OUTB_LSD2									OUTG_LSD2						
R-0h									R-0h						
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
OUTG_LSD2				OUTR_LSD2											→

R-0h										R-0h						→
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
OUTB_LSD1										OUTG_LSD1						
R-0h										R-0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OUTG_LSD1					OUTR_LSD1											
R-0h					R-0h											

Table 31. SID Register Field Descriptions

Bit	Field	Type	Default	Description
176–166	OUTB_LOD2[10:0]	R	0h	LOD2 for OUTB10–OUTB0. For each channel: 0h = No fault detected 1h = Fault detected
165–155	OUTG_LOD2[10:0]	R	0h	LOD2 for OUTG10–OUTG0. For each channel: 0h = No fault detected 1h = Fault detected
154–144	OUTR_LOD2[10:0]	R	0h	LOD2 for OUTR10–OUTR0. For each channel: 0h = No fault detected 1h = Fault detected
143–133	OUTB_LOD1[10:0]	R	0h	LOD1 for OUTB10–OUTB0. For each channel: 0h = No fault detected 1h = Fault detected
132–122	OUTG_LOD1[10:0]	R	0h	LOD1 for OUTG10–OUTG0. For each channel: 0h = No fault detected 1h = Fault detected
121–111	OUTR_LOD1[10:0]	R	0h	LOD1 for OUTR10–OUTR0. For each channel: 0h = No fault detected 1h = Fault detected
110–100	OUTB_APS[10:0]	R	0h	APS status for OUTB10–OUTB0. For each channel: 0h = No fault detected 1h = Fault detected
99–89	OUTG_APS[10:0]	R	0h	APS status for OUTG10–OUTG0. For each channel: 0h = No fault detected 1h = Fault detected
88–78	OUTR_APS[10:0]	R	0h	APS status for OUTR10–OUTR0. For each channel: 0h = No fault detected 1h = Fault detected
77	TEF	R	0h	Thermal error flag 0h = No fault detected 1h = Fault detected

76	PTW	R	0h	Pre-thermal warning flag 0h = No fault detected 1h = Fault detected
75–73	APS_FLAG[2:0]	R	0h	APS test flag fault 3h = APS test passes 6h = APS test fails
72	ISF	R	0h	ISF fault 0h = No fault detected 1h = Fault detected
71	IOF	R	0h	IOF fault 0h = No fault detected 1h = Fault detected
70–68	LOD_LSD_FLAG[2:0]	R	0h	LOD_LSD self-test flag 3h = LOD_LSD self-test passes 6h = LOD_LSD self-test fails
67	NEG1	R	0h	Neg1 bit value
66	NEG0	R	0h	Neg0 bit value
65–55	OUTB_LSD2[10:0]	R	0h	LSD2 for OUTB10–OUTB0. For each channel: 0h = No fault detected 1h = Fault detected
54–44	OUTG_LSD2[10:0]	R	0h	LSD2 for OUTG10–OUTG0. For each channel: 0h = No fault detected 1h = Fault detected
43–33	OUTR_LSD2[10:0]	R	0h	LSD2 for OUTR10–OUTR0. For each channel: 0h = No fault detected 1h = Fault detected
32–22	OUTB_LSD1[10:0]	R	0h	LSD1 for OUTB10–OUTB0. For each channel: 0h = No fault detected 1h = Fault detected
21–11	OUTG_LSD1[10:0]	R	0h	LSD1 for OUTG10–OUTG0. For each channel: 0h = No fault detected 1h = Fault detected
10–0	OUTR_LSD1[10:0]	R	0h	LSD1 for OUTR10–OUTR0. For each channel: 0h = No fault detected 1h = Fault detected