HT6000 Series – HT6122E (Evaluation Version)

High Efficiency, Dual Buck DC-DC Controller with Internal Protocol, Selectable Switching Frequency up to 350kHz

APPLICATION

- USB Type-C/Type-A fast charging applications
- LCD monitor/TV
- Desktop PC
- Automotive ADAS Power
- Low EMI Application (Patent Pending)

GENERAL DESCRIPTION

HT6122E is an easy to use, high efficiency, dual-channel, synchronous step-down switching controller designed for high-power dual ports fast charging applications. It has one channel built in QC Protocol for easy configuration to one Type-A and one Type-C fast charging output. With one channel of Type A fast charging, another channel is flexible to be used as a general-purpose DC-DC applications, fitting different needs of users' requirements.

HT6122E has a wide input voltage range from 4.7V to 16V, supports output voltages from 3.6V to 15V with typical current of 3A, the switching frequency is selectable to cover wide range of applications.

HT6122E has soft start function, which can prevent the inrush current at startup from affecting the stability of the input power.

HT6122E has a variety of protection, such as input overvoltage protection, undervoltage protection, output over current protection, overvoltage, undervoltage, short circuit protection, and etc.

FEATURES

Dual-Channel Synchronous Buck Controller

- Wide input voltage range: 4.7V to 16V
- Output current up to 3A, or higher
- One channel built in QC Protocol, reducing BOM
- External feedback for another channel
- Dual Channel Fast Charging simultaneously
- Selectable switching frequency at 150kHz, 250kHz and 350kHz
- Support CC / CV mode
- Soft start

Multi-Protection

- Input under-voltage lockout (UVLO)
- Output over-voltage protection (OVP)
- Output short-circuit protection (SCP)
- Over-temperature protection (OTP)

DEVICE INFORMATION

Part Number	Package	Dimensions (mm)
HT6122E	WQFN32	5.0 x 5.0 x 0.75

See package outline and dimensions on page 10.

Typical Application Circuit

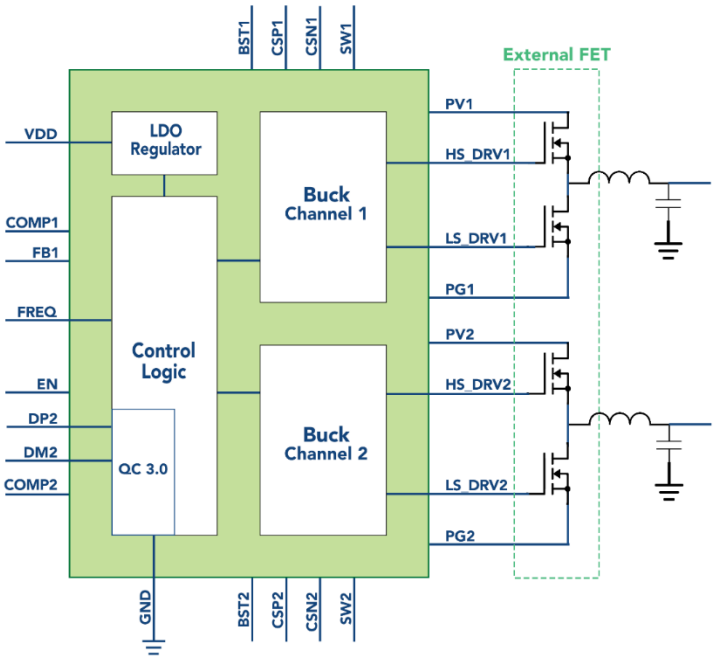


Fig. 1.1 – HT6122E Application Circuit

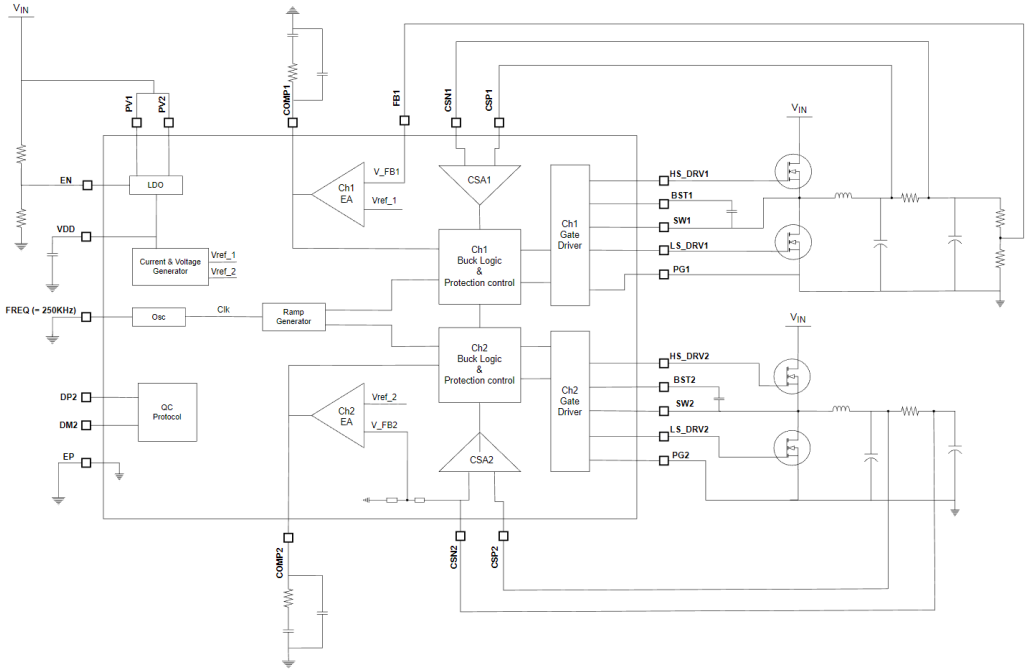


Fig. 1.2 – Detailed HT6122E Application Circuit

Pin Configuration

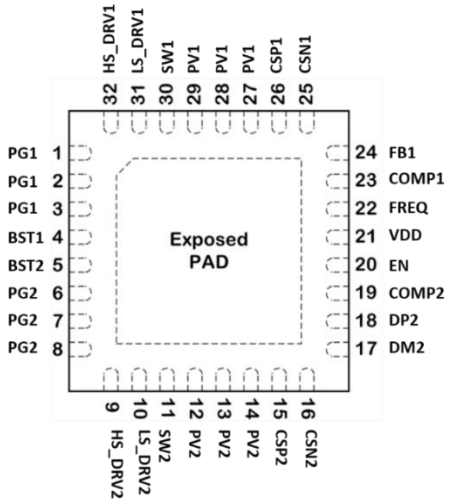


Fig. 2 - 32-pin QFN, 5x5 mm^2, 0.5mm pitch TOP VIEW

Pin Functions

Pin	Name	Description	Pin	Name	Description
1	PG1	Power Ground Channel 1	**17**	DM2	USB D- channel 2
2	PG1		**18**	DP2	USB D+ channel 2
3	PG1		**19**	COMP2	Compensation Pin 2
4	BST1	Bootstrap Channel 1, Connect a capacitor (recommended 0.1uF) to SW1.	**20**	EN	Chip Enable, 1.35V enables the device
5	BST2	Bootstrap Channel 2, Connect a capacitor (recommended 0.1uF) to SW2.	**21**	VDD	VDD Regulator Connect a decoupling capacitor to GND. Recommended 2.2uF.
6	PG2	Power Ground Channel 2	**22**	FREQ	Frequency Selection, See Application Information Section for detail
7	PG2		**23**	COMP1	Compensation Pin 1
8	PG2		**24**	FB1	Feedback Pin 1
9	HS_DRV2	High Side Gate Drive Channel 2	**25**	CSN1	Current Sense Negative 1
10	LS_DRV2	Low Side Gate Drive Channel 2	**26**	CSP1	Current Sense Positive 1
11	SW2	Inductor Connection Channel 2	**27**	PV1	Input Power Channel 1, Connect a capacitor (recommended 1uF) to PV1.
12	PV2	Input Power Channel 2, Connect a capacitor (recommended 1uF) to PV2.	**28**	PV1	
13	PV2		**29**	PV1	
14	PV2		**30**	SW1	Inductor Connection Channel 1
15	CSP2	Current Sense Positive 2	**31**	LS_DRV1	Low Side Gate Drive Channel 1
16	CSN2	Current Sense Negative 2	**32**	HS_DRV1	High Side Gate Drive Channel 1
33	EPAD	Signal Ground and Thermal Dissipation Pad			

Absolute Maximum Ratings

PV1, PV2, SW1, SW2, EN	-0.3V to 18V
HS_DRV1, HS_DRV2, BST1, BST2	-0.3V to 20V
LS_DRV1, LS_DRV2	-0.3V to 6V
CSP1, CSN1, CSP2, CSN2	-0.3V to 18V
VDD, COMP1, COMP2, FB1, FREQ, DP2, DM2	-0.3V to 6V
Operating Temperature Range	-40°C to 85°C
Maximum Junction Temperature	-40°C to 125°C
Storage Temperature Range	-65°C to 125°C
Soldering Temperature	300°C

Electrical Characteristics (TA=25°C unless specified)

Parameters	Symbol	Test Conditions	Rating			Unit
			MIN	TYP	MAX	
Input Characteristics						
Operating Input Supply Voltage	V_{IN}		4.7		16	V
EN Threshold	V_{EN}			1.35		V
EN Hysteresis	V_{ENHYS}			110		mV
Quiescent Current	I_Q	Output at no load		1.5		mA
Shutdown Current	I_{stb}	VEN = 0V		10		μA
Output Characteristics*						
Channel 1 Output Voltage Range	V_{OUT1}	V_{IN} = 16V	3.6		15	V
Channel 1 Output Current Limit	I_{Limit_FB}	R_{SENSE} = 10mΩ		3.3		A
Channel 2 Output Voltage (QC3)	V_{OUT2_QC3}	QC5V: D+ = 0.6V, D- = 0V		5		V
		QC9V: D+ = 3.3V, D- = 0.6V		9		V
		QC12V: D+ = 0.6V, D- = 0.6V		12		V
	V_{STEP_QC3}	Cont.Mode: D+ = 0.6V, D- = 3.3V		200		mV
Channel 2 Output Current Limit (QC3)	I_{Limit_QC3}	R_{SENSE} = 10 mΩ, V_{OUT2}=5V		3		A
		R_{SENSE} = 10 mΩ, V_{OUT2}=9V		2		A
		R_{SENSE} = 10 mΩ, V_{OUT2}=12V		1.5		A
Channel 2 Fixed Cable Compensation Voltage	V_{CABLE}	V_{OUT2} = 5V, I_{OUT2}=3A		450		mV
Reference Voltage						
Output Voltage Reference	V_{FB}	Measured at FB1, FB2		1		V
Regulator Reference	V_{DD}	Measured at VDD		5.4		V
Switching Characteristics						
Switching Frequency	f_{sw}	FREQ=Z		150		kHz
		FREQ=L		250		kHz
		FREQ=H		350		kHz
Minimum On-Time	$t_{ON, Min}$			80		ns

*Output load startup threshold = 1.5A

Electrical Characteristics (T_A=25°C unless specified)

Parameters	Symbol	Test Conditions	Rating			Unit
			MIN	TYP	MAX	
Dither Generator						
Dither Modulation Frequency	f_{DITH}			TBD		kHz
Maximum Switching Frequency	f_{OSCMAX}			TBD		kHz
Minimum Switching Frequency	f_{OSCMIN}			TBD		kHz
Input Under-voltage Lockout						
Input Under-Voltage Lockout Threshold	V_{UVLO}			4.7		V
Input Under-Voltage Lockout Hysteresis	V_{UVHYS}		0.53	0.64	0.71	V
Output Under-voltage Lockout						
Output Under-voltage Protection	V_{UVLO}			V_{OUT}*60%		V
Output Over-voltage Protection						
Over-Voltage Protection	V_{OVP}			V_{OUT}*120%		V
Over-Temperature Protection						
Thermal Shutdown	T_{SD}	Increasing Temperature		140		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}	Decreasing temperature		30		°C

Functional Block Diagram

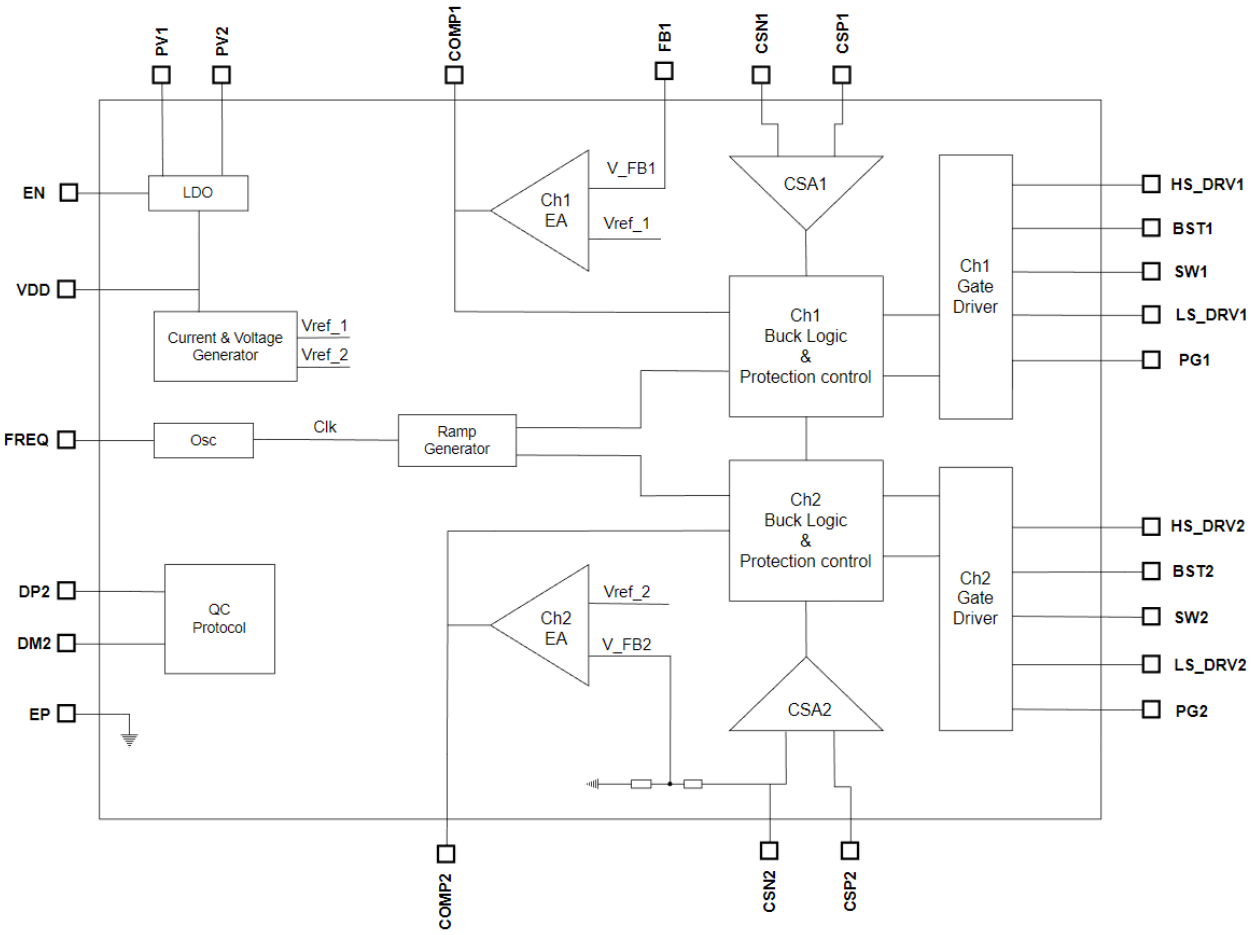


Fig. 3 – Functional Block Diagram

Application Information

Input Protection

If the input voltage is smaller than the Input UVLO, both buck channels stop the gate driver, reset and enter hiccup mode. It returns to Normal when the faults are cleared.

Output Protection

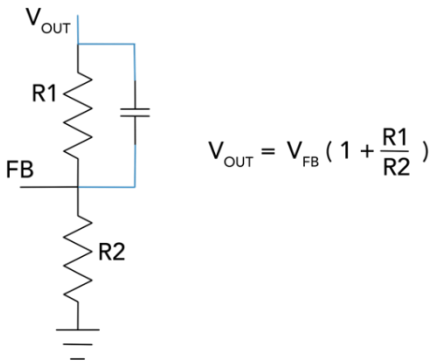
The Output Under-voltage Lockout threshold and the Output Over-voltage Protection are set at V_{OUT}*60% and V_{OUT}*120%. Once Output UVLO or OVP is triggered, the specific channel stops the gate driver, reset and enters hiccup mode.

Soft Start

HT6000 series employs an internal soft start in the buck converter to prevent large inrush current and overshoots of V_{OUT}. The soft start time is 20ms in the design.

Feedback and Output Voltage

HT6122E provides an external FB for setting the output voltage. Usually, feedback resistor divider tap is connected and V_{FB} is regulated at 1V. The relationship between the V_{OUT} and the resistor divider tap is as follows:



$$V_{OUT} = V_{FB}\left(1 + \frac{R1}{R2}\right)$$

Fig. 4 – Feedback Resistor Network Design

Frequency Selection

The switching frequency can be selected by applying different condition to the pin FREQ.

FREQ state	f_{sw} (kHz)
Z	150
L	250
H (Tied to VDD)	350

The efficiency of the conversion depends on the switching FET. Usually, the efficiency is higher at lower frequency because of lower switching loss.

Efficiency and External FET R_{dson}

The accuracy of the output voltage and the conversion efficiency is highly affected by the R_{dson} of the external FET. The lower the R_{dson} the higher the efficiency and voltage accuracy.

Constant Voltage / Constant Current Mode

HT6122E has the capability to operate in either CV (constant voltage) mode or CC (constant current) mode, with a smooth transition from CV to CC (See Fig.5). When in CV mode, it regulates the output voltage. Once the output current limit threshold is reached, HT6122E switches to CC mode. In CC mode, the output voltage decreases while the output current remains clamped at the predefined values. The current limit can be determined using the following equation.

$$I_{out(\max)} = \frac{33mV}{R_{sense}}$$

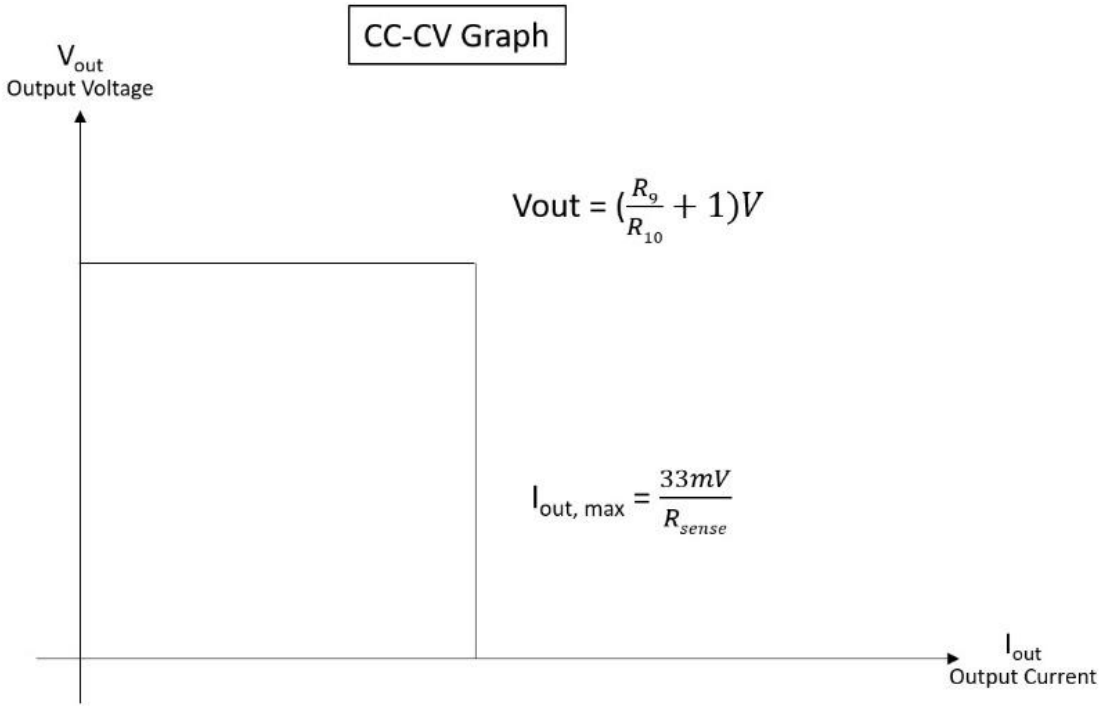


Fig. 5 - CC-CV Graph

Typical Application Schematic

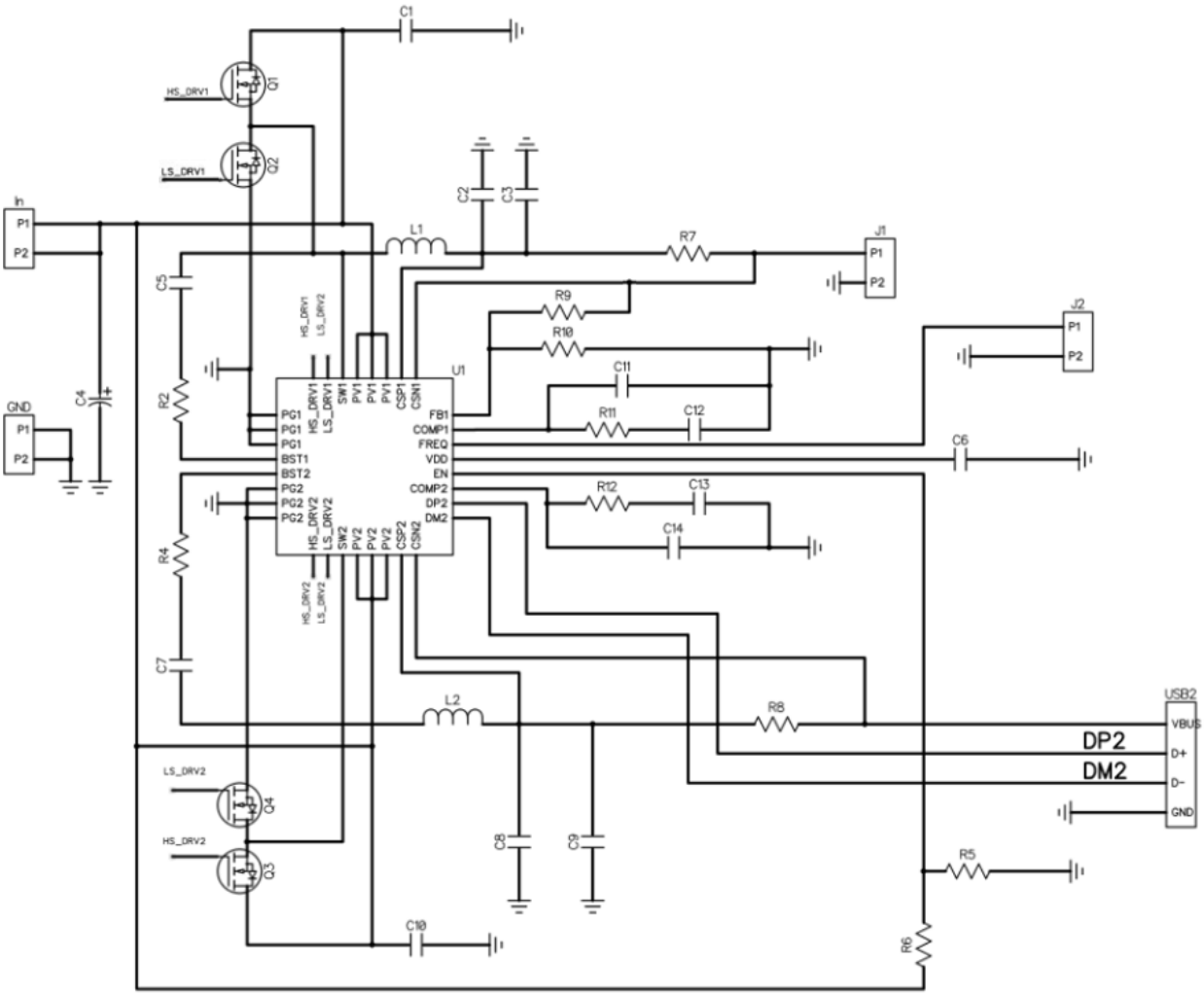
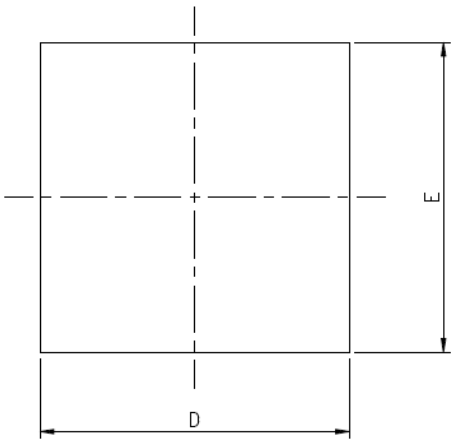


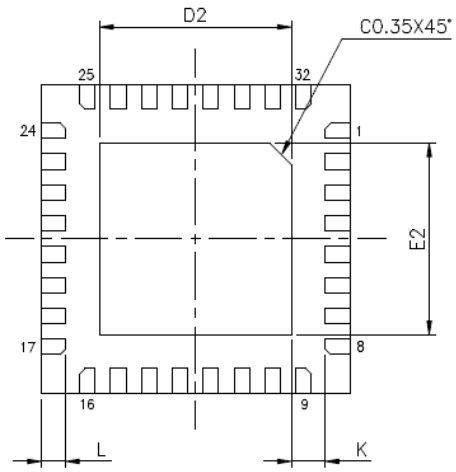
Fig. 6 - HT6122E application schematic diagram

Package Outline and Dimensions

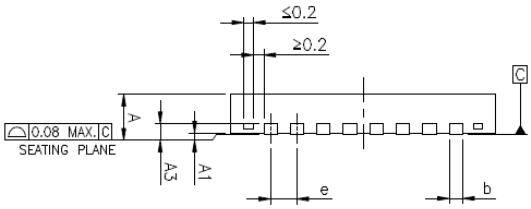
32-pin QFN (5mm x 5mm, 0.5mm pitch)



Top View



Bottom



Side View

	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X532)			VQFN(Y532)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
b	0.18	0.25	0.30	0.18	0.25	0.30
D	5.00 BSC			5.00 BSC		
E	5.00 BSC			5.00 BSC		
e	0.50 BSC			0.50 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	—	—	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Dual Ports MAX SPEED

HT6000 Series

Fast Charging is just a Breeze

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